



Q67H2-AD/ Q65H2-AD/ H67H2-AD

Rev : 1.0

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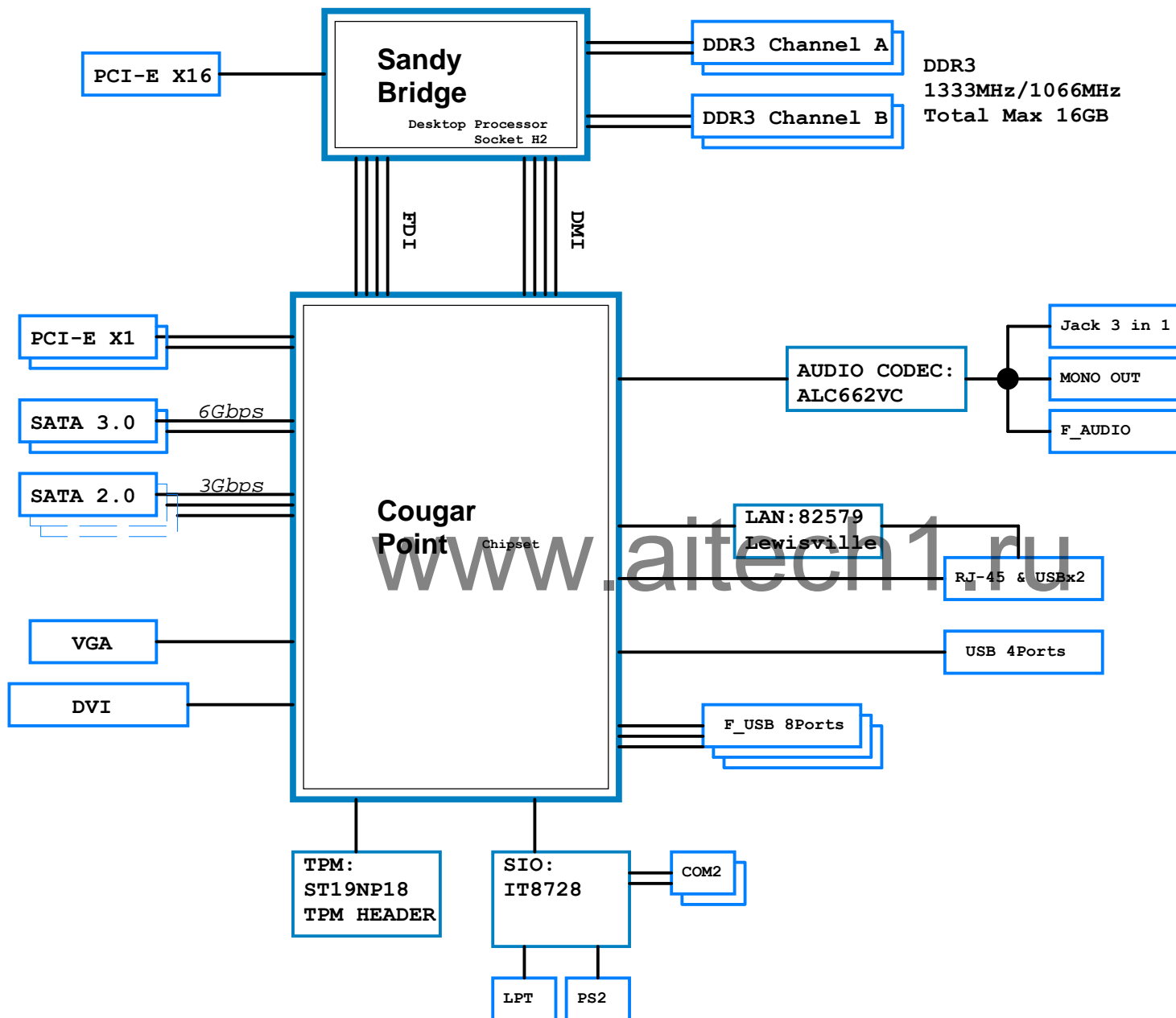
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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/22	Initial version
V.B	2010/08/24	
V.C	2010/09/10	
V.1.0	2010/09/16	

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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	LPT Detect	GPI
GPIO22	VCC3	CLR_CMOS	GPI
GPIO38	VCC3	KM Detect	GPI
GPIO39	VCC3	SENSE_Header	GPI
GPIO48	VCC3	SENSE_Header	GPI
GPIO21	VCC3	COM2 Detect	GPI
GPIO36	VCC3	TCM,TPM Detect	GPI
GPIO37	VCC3	TCM,TPM Detect	GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

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9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
9 M_MA_A[0..15]	← M_MA A[0..15]
9 M_BS_A[0..2]	← M_BS A[0..2]
9 M_CS_A_L[0..3]	← M_CS A_L[0..3]
9 M_CKE_A[0..3]	← M_CKE A[0..3]
9 M_ODT_A[0..3]	← M_ODT A[0..3]
9 M_CLK_A_P[0..3]	← M_CLK A_P[0..3]
9 M_CLK_A_N[0..3]	← M_CLK A_N[0..3]
9 M_WE_A_L	← M_WE A_L
9 M_CAS_A_L	← M_CAS A_L
9 M_RAS_A_L	← M_RAS A_L

DDR3 CH.A

9,10 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
10 M_MA_B[0..15]	← M_MA B[0..15]
10 M_BS_B[0..2]	← M_BS B[0..2]
10 M_CS_B_L[0..3]	← M_CS B_L[0..3]
10 M_CKE_B[0..3]	← M_CKE B[0..3]
10 M_ODT_B[0..3]	← M_ODT B[0..3]
10 M_CLK_B_P[0..3]	← M_CLK B_P[0..3]
10 M_CLK_B_N[0..3]	← M_CLK B_N[0..3]
10 M_WE_B_L	← M_WE B_L
10 M_CAS_B_L	← M_CAS B_L
10 M_RAS_B_L	← M_RAS B_L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_DQ_4
M_DATA_A5	AJ1	SA_DQ_5
M_DATA_A6	AL1	SA_DQ_6
M_DATA_A7	AL2	SA_DQ_7
M_DATA_A8	AN1	SA_DQ_8
M_DATA_A9	AN4	SA_DQ_9
M_DATA_A10	AR3	SA_DQ_10
M_DATA_A11	AR4	SA_DQ_11
M_DATA_A12	AN2	SA_DQ_12
M_DATA_A13	AR2	SA_DQ_13
M_DATA_A14	AR1	SA_DQ_14
M_DATA_A15	SA_DQ_15	
M_DATA_A16	AV2	SA_DQ_16
M_DATA_A17	AW3	SA_DQ_17
M_DATA_A18	AV5	SA_DQ_18
M_DATA_A19	AU2	SA_DQ_19
M_DATA_A20	AU3	SA_DQ_20
M_DATA_A21	AU5	SA_DQ_21
M_DATA_A22	AV5	SA_DQ_22
M_DATA_A23	AV5	SA_DQ_23
M_DATA_A24	AU7	SA_DQ_24
M_DATA_A25	AU7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU9	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AW7	SA_DQ_29
M_DATA_A30	AU9	SA_DQ_30
M_DATA_A31	AY9	SA_DQ_31
M_DATA_A32	AU35	SA_DQ_32
M_DATA_A33	AW37	SA_DQ_33
M_DATA_A34	AU39	SA_DQ_34
M_DATA_A35	AW35	SA_DQ_35
M_DATA_A36	AY36	SA_DQ_36
M_DATA_A37	AU38	SA_DQ_37
M_DATA_A38	AU37	SA_DQ_38
M_DATA_A39	AU37	SA_DQ_39
M_DATA_A40	AR37	SA_DQ_40
M_DATA_A41	AN36	SA_DQ_41
M_DATA_A42	AN37	SA_DQ_42
M_DATA_A43	AR39	SA_DQ_43
M_DATA_A44	AR38	SA_DQ_44
M_DATA_A45	AN38	SA_DQ_45
M_DATA_A46	AN40	SA_DQ_46
M_DATA_A47	AL40	SA_DQ_47
M_DATA_A48	AL37	SA_DQ_48
M_DATA_A49	AJ38	SA_DQ_49
M_DATA_A50	AJ37	SA_DQ_50
M_DATA_A51	AJ38	SA_DQ_51
M_DATA_A52	AJ38	SA_DQ_52
M_DATA_A53	AJ39	SA_DQ_53
M_DATA_A54	AJ40	SA_DQ_54
M_DATA_A55	AG40	SA_DQ_55
M_DATA_A56	AG37	SA_DQ_56
M_DATA_A57	AE38	SA_DQ_57
M_DATA_A58	AE37	SA_DQ_58
M_DATA_A59	AG39	SA_DQ_59
M_DATA_A60	AG38	SA_DQ_60
M_DATA_A61	AE39	SA_DQ_61
M_DATA_A62	AE38	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7
M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW8	SA_DQS#_3
M_DQS_A_N4	AV38	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

SM_DRAMRST#

SA_DQS_8

SA_DQS#_8

SA_ECC_CB_0

SA_ECC_CB_1

SA_ECC_CB_2

SA_ECC_CB_3

SA_ECC_CB_4

SA_ECC_CB_5

SA_ECC_CB_6

SA_ECC_CB_7

DDR_0

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SKT_H2_CRB

DDR3 CH.A

AV27	M_MA_A0
AV24	M_MA_A1
AW24	M_MA_A2
AW23	M_MA_A3
AV23	M_MA_A4
AT24	M_MA_A5
AT23	M_MA_A6
AJ22	M_MA_A7
AV22	M_MA_A8
AT22	M_MA_A9
AV28	M_MA_A10
AJ21	M_MA_A11
AT21	M_MA_A12
AW22	M_MA_A13
AJ20	M_MA_A14
AT20	M_MA_A15

AW29	M_WE_A_L
AW30	M_CAS_A_L
AJ28	M_RAS_A_L

AY29	M_BS_A0
AW28	M_BS_A1
AV20	M_BS_A2

AJ29	M_CS_A_L0
AW30	M_CS_A_L1
AJ33	M_CS_A_L3

AV19	M_CKE_A0
AT19	M_CKE_A1
AJ18	M_CKE_A2
AV18	M_CKE_A3

AY31	M_ODT_A0
AJ32	M_ODT_A1
AW30	M_ODT_A2
AW33	M_ODT_A3

AY25	M_CLK_A_P0
AW25	M_CLK_A_N0
AJ24	M_CLK_A_P1
AW25	M_CLK_A_N1
AY27	M_CLK_A_P2
AV26	M_CLK_A_P3
AW26	M_CLK_A_N3

AW18DDR3_DRAMRST_L

AV13

AV12

AJ12

AJ14

AW13

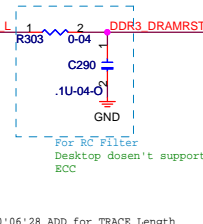
AY13

AJ13

AJ14

AY12

AW12



Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B13	AL7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B11	AM10	SB_DQ_10
M_DATA_B15	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B8	AM6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B10	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AR7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AR9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AL13	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
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M_DATA_B41	AP31	SB_DQ_41
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M_DATA_B50	AL34	SB_DQ_55
M_DATA_B56	AH35	SB_DQ_56
M_DATA_B57	AH34	SB_DQ_57
M_DATA_B58	AE34	SB_DQ_58
M_DATA_B59	AE35	SB_DQ_59
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M_DATA_B61	AJ34	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

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M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN3	SB_DQS_3
M_DQS_B_P4	AN3	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN28	SB_DQS#_4
M_DQS_B_N5	AR32	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

CPU1D

SB_DQ_0	AK24	M_MA_B0
SB_DQ_1	AM20	M_MA_B1
SB_DQ_2	AM19	M_MA_B2
SB_DQ_3	AK18	M_MA_B3
SB_DQ_4	AP19	M_MA_B4
SB_DQ_5	AP18	M_MA_B5
SB_DQ_6	AM18	M_MA_B6
SB_DQ_7	AL18	M_MA_B7
SB_DQ_8	AN18	M_MA_B8
SB_DQ_9	AY17	M_MA_B9
SB_DQ_10	AN23	M_MA_B10
SB_DQ_11	AJ17	M_MA_B11
SB_DQ_12	AT18	M_MA_B12
SB_DQ_13	AR26	M_MA_B13
SB_DQ_14	AY16	M_MA_B14
SB_DQ_15	AV16	M_MA_B15
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SB_DQS_7

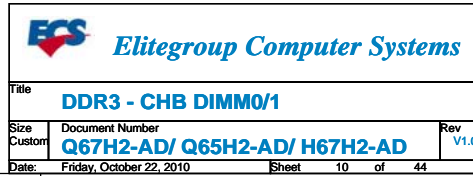
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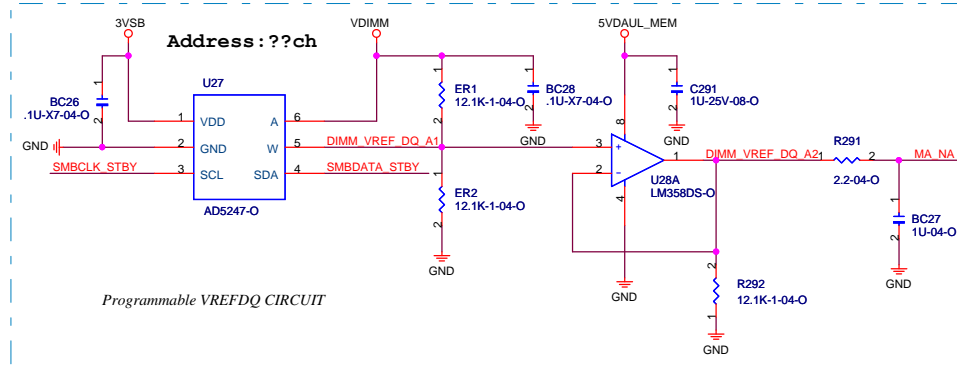
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SB_DQ_3	AK18	M_MA_B3
SB_DQ_4	AP19	M_MA_B4
SB_DQ_5	AP18	M_MA_B5
SB_DQ_6	AM18	M_MA_B6
SB_DQ_7	AL18	M_MA_B7
SB_DQ_8	AN18	M_MA_B8
SB_DQ_9	AY17	M_MA_B9
SB_DQ_10	AN23	M_MA_B10
SB_DQ_11	AJ17	M_MA_B11
SB_DQ_12	AT18	M_MA_B12
SB_DQ_13	AR26	M_MA_B13
SB_DQ_14	AY16	M_MA_B14
SB_DQ_15	AV16	M_MA_B15
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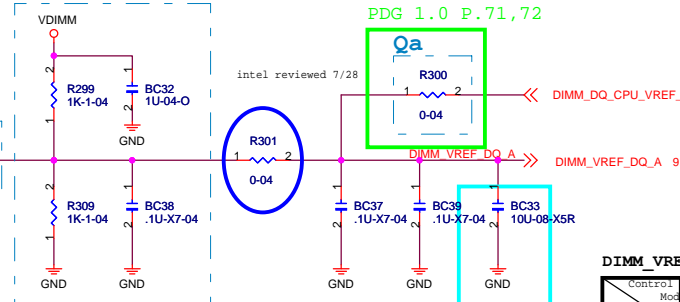
CPU1I				CPU1J			
BALLMAP_REV=1.4				BALLMAP_REV=1.4			
A17	VSS_001	VSS_091	AM27	AV11	VSS_181	VSS_271	G8
A23	VSS_002	VSS_092	AM3	AV14	VSS_182	VSS_272	H1
A26	VSS_003	VSS_093	AM30	AV17	VSS_183	VSS_273	H17
A29	VSS_004	VSS_094	AM36	AV3	VSS_184	VSS_274	H2
A35	VSS_005	VSS_095	AM37	AV35	VSS_185	VSS_275	H20
AA33	VSS_006	VSS_096	AM38	AV38	VSS_186	VSS_276	H22
AA34	VSS_007	VSS_097	AM39	AV6	VSS_187	VSS_277	H23
AA35	VSS_008	VSS_098	AM4	AW10	VSS_188	VSS_278	H29
AA36	VSS_009	VSS_099	AM40	AW11	VSS_189	VSS_279	H33
AA37	VSS_010	VSS_100	AM5	AW14	VSS_190	VSS_280	H35
AA38	VSS_011	VSS_101	AN10	AW16	VSS_191	VSS_281	H37
AB5	VSS_012	VSS_102	AN11	AW36	VSS_192	VSS_282	H39
AC1	VSS_013	VSS_103	AN17	AY11	VSS_193	VSS_283	H5
AC1	VSS_014	VSS_104	AN19	AY14	VSS_194	VSS_284	H6
AC6	VSS_015	VSS_105	AN22	AY18	VSS_195	VSS_285	H9
AD33	VSS_016	VSS_106	AN24	AY35	VSS_196	VSS_286	J17
AD36	VSS_017	VSS_107	AN27	AY4	VSS_197	VSS_287	J20
AD38	VSS_018	VSS_108	AN30	AY6	VSS_198	VSS_288	J23
AD39	VSS_019	VSS_109	AN31	AY8	VSS_199	VSS_289	J26
AD40	VSS_020	VSS_110	AN32	B10	VSS_200	VSS_290	J29
AD5	VSS_021	VSS_111	AN33	B13	VSS_201	VSS_291	J32
AD8	VSS_022	VSS_112	AN34	B14	VSS_202	VSS_292	K1
AE3	VSS_023	VSS_113	AN35	B17	VSS_203	VSS_293	K12
AE33	VSS_024	VSS_114	AN36	B23	VSS_204	VSS_294	K13
AE36	VSS_025	VSS_115	AN5	B26	VSS_205	VSS_295	K13
AF1	VSS_026	VSS_116	AN6	B29	VSS_206	VSS_296	K14
AF34	VSS_027	VSS_117	AN7	B32	VSS_207	VSS_297	K17
AF36	VSS_028	VSS_118	AN8	B35	VSS_208	VSS_298	K2
AF37	VSS_029	VSS_119	AN9	B38	VSS_209	VSS_299	K20
AF40	VSS_030	VSS_120	AP1	B6	VSS_210	VSS_300	K23
AF5	VSS_031	VSS_121	AP11	C11	VSS_211	VSS_301	K26
AF6	VSS_032	VSS_122	AP14	C12	VSS_212	VSS_302	K29
AF7	VSS_033	VSS_123	AP17	C17	VSS_213	VSS_303	K33
AG36	VSS_034	VSS_124	AP22	C20	VSS_214	VSS_304	K34
AH2	VSS_035	VSS_125	AP25	C23	VSS_215	VSS_305	K35
AH3	VSS_036	VSS_126	AP27	C26	VSS_216	VSS_306	K37
AH33	VSS_037	VSS_127	AP30	C29	VSS_217	VSS_307	K5
AH36	VSS_038	VSS_128	AP36	C32	VSS_218	VSS_308	K6
AH37	VSS_039	VSS_129	AP36	C35	VSS_219	VSS_309	L10
AH38	VSS_040	VSS_130	AP4	C7	VSS_220	VSS_310	L17
AH40	VSS_041	VSS_131	AP40	C8	VSS_221	VSS_311	L20
AH5	VSS_042	VSS_132	AP5	D17	VSS_222	VSS_312	L23
AH8	VSS_043	VSS_133	AR11	D2	VSS_223	VSS_313	L26
AH12	VSS_044	VSS_134	AR14	D22	VSS_224	VSS_314	L29
AH15	VSS_045	VSS_135	AR17	D23	VSS_225	VSS_315	M1
AH18	VSS_046	VSS_136	AR18	D26	VSS_226	VSS_316	M17
AJ21	VSS_047	VSS_137	AR19	D29	VSS_227	VSS_317	M2
AJ25	VSS_048	VSS_138	AR27	D32	VSS_228	VSS_318	M20
AJ27	VSS_049	VSS_139	AR30	D37	VSS_229	VSS_319	M23
AJ36	VSS_050	VSS_140	AR36	D38	VSS_230	VSS_320	M26
AJ5	VSS_051	VSS_141	AT1	D4	VSS_231	VSS_321	M3
AK1	VSS_052	VSS_142	AT5	D5	VSS_232	VSS_322	M33
AK10	VSS_053	VSS_143	AT10	D9	VSS_233	VSS_323	M35
AK13	VSS_054	VSS_144	AT12	E11	VSS_234	VSS_324	M37
AK14	VSS_055	VSS_145	AT13	E12	VSS_235	VSS_325	M39
AK16	VSS_056	VSS_146	AT15	E17	VSS_236	VSS_326	M5
AK22	VSS_057	VSS_147	AT16	E20	VSS_237	VSS_327	M6
AK28	VSS_058	VSS_148	AT17	E23	VSS_238	VSS_328	M9
AK31	VSS_059	VSS_149	AT2	E26	VSS_239	VSS_329	N8
AK32	VSS_060	VSS_150	AT25	E29	VSS_240	VSS_330	P1
AK33	VSS_061	VSS_151	AT27	E32	VSS_241	VSS_331	P2
AK34	VSS_062	VSS_152	AT28	E36	VSS_242	VSS_332	P36
AK35	VSS_063	VSS_153	AT29	F7	VSS_243	VSS_333	P38
AK36	VSS_064	VSS_154	AT3	E8	VSS_244	VSS_334	P40
AK37	VSS_065	VSS_155	AT3	F8	VSS_245	VSS_335	P40
AK37	VSS_066	VSS_156	AT30	F10	VSS_246	VSS_336	P5
AK4	VSS_067	VSS_157	AT31	F13	VSS_247	VSS_337	P33
AK40	VSS_068	VSS_158	AT32	F14	VSS_248	VSS_338	R35
AK5	VSS_069	VSS_159	AT33	F17	VSS_249	VSS_339	R37
AK6	VSS_070	VSS_160	AT34	F19	VSS_250	VSS_340	R37
AK7	VSS_071	VSS_161	AT35	F2	VSS_251	VSS_341	R39
AK8	VSS_072	VSS_162	AT36	F20	VSS_252	VSS_342	T1
AK9	VSS_073	VSS_163	AT37	F23	VSS_253	VSS_343	T5
AL11	VSS_074	VSS_164	AT38	F26	VSS_254	VSS_344	T6
AL14	VSS_075	VSS_165	AT39	F29	VSS_255	VSS_345	U8
AL17	VSS_076	VSS_166	AT4	F35	VSS_256	VSS_346	V1
AL19	VSS_077	VSS_167	AT40	F37	VSS_257	VSS_347	V2
AL24	VSS_078	VSS_168	AT41	F39	VSS_258	VSS_348	V3
AL27	VSS_079	VSS_169	AT42	F5	VSS_259	VSS_349	V4
AL30	VSS_080	VSS_170	AT43	F6	VSS_259	VSS_349	V4
AL36	VSS_080	VSS_170	AT7	F38	VSS_258	VSS_348	V3
AL5	VSS_081	VSS_171	AT8	F9	VSS_260	VSS_350	V35
AM1	VSS_082	VSS_172	AT9	G11	VSS_261	VSS_351	V36
AM1	VSS_083	VSS_173	AT9	G11	VSS_262	VSS_352	V36
AM11	VSS_084	VSS_174	AT15	G12	VSS_263	VSS_353	V37
AM14	VSS_085	VSS_175	AT15	G12	VSS_264	VSS_354	V37
AM17	VSS_086	VSS_176	AT15	G12	VSS_264	VSS_354	V37
AM2	VSS_086	VSS_176	AT15	G12	VSS_264	VSS_354	V37
AM2	VSS_087	VSS_177	AT15	G12	VSS_264	VSS_354	V37
AM21	VSS_088	VSS_178	AT15	G12	VSS_264	VSS_354	V37
AM23	VSS_089	VSS_179	AT15	G12	VSS_264	VSS_354	V37
AM25	VSS_090	VSS_180	AV10	G7	VSS_270	VSS_360	Y8
A4	VSS_NCTF_01			AY37	VSS_NCTF_03		
AV39	VSS_NCTF_02			B3	VSS_NCTF_04		
9 OF 10				10 OF 10			



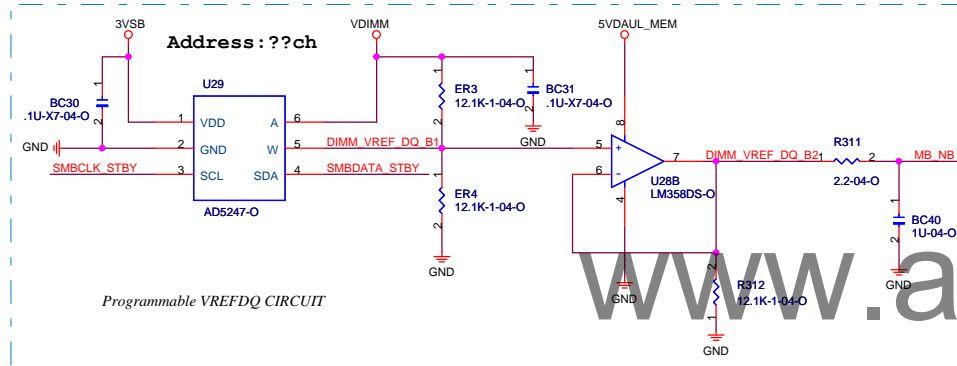
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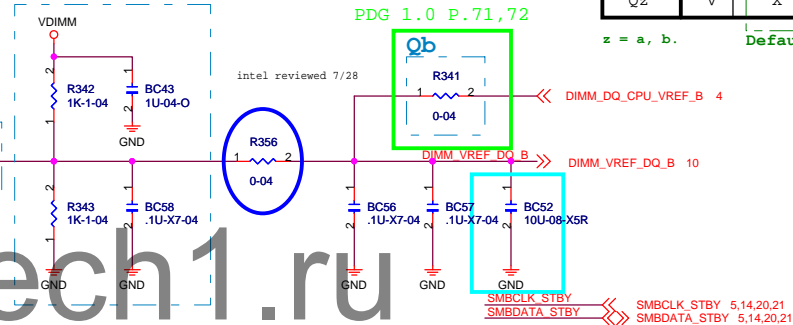
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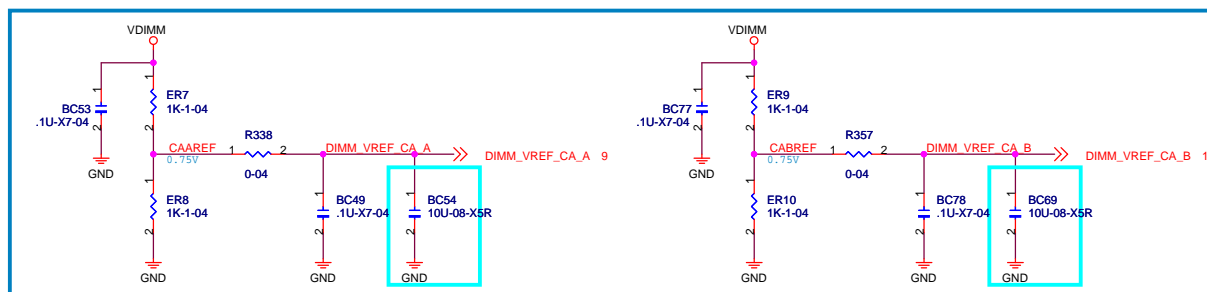
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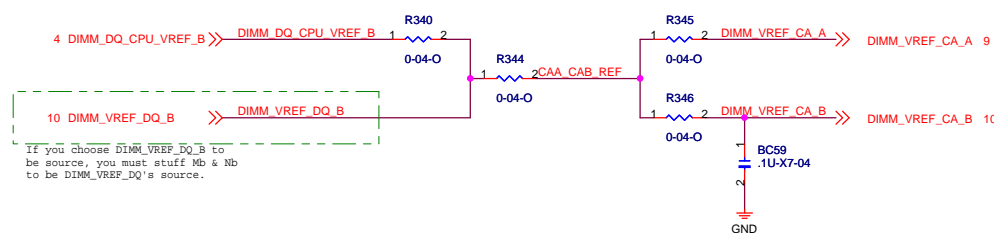
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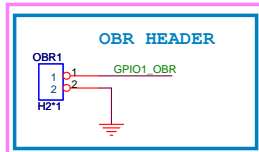


DIMM_VREF_DQ Control Circuit

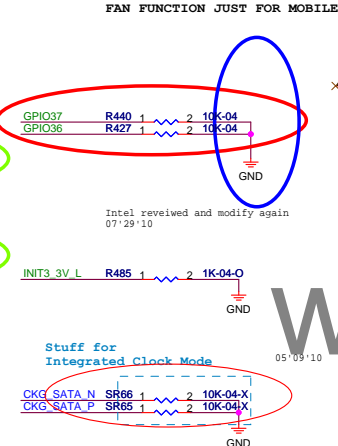
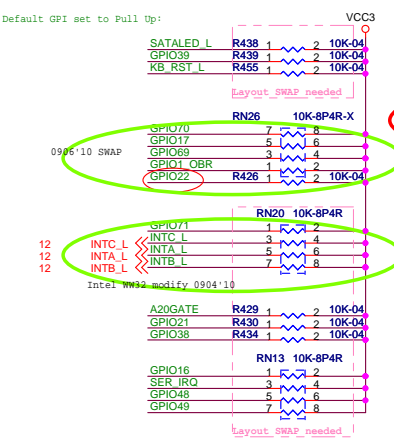
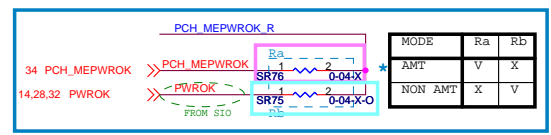


DIMM_VREF_CA Circuit





Q67/Q65 上件
H67 上件



MOBILE ONLY, NOT FOR DESKTOP.
CRB CONNECT TO MINI PCIe.

GPIO17 BT17
GPIO18 BR19
GPIO19 BT21
GPIO20 BM20
GPIO21 BN19
GPIO22 BA53
GPIO23 BE54
GPIO24 BF55
GPIO25 AW53
GPIO26
GPIO27
GPIO28
GPIO29
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
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GPIO99
GPIO100

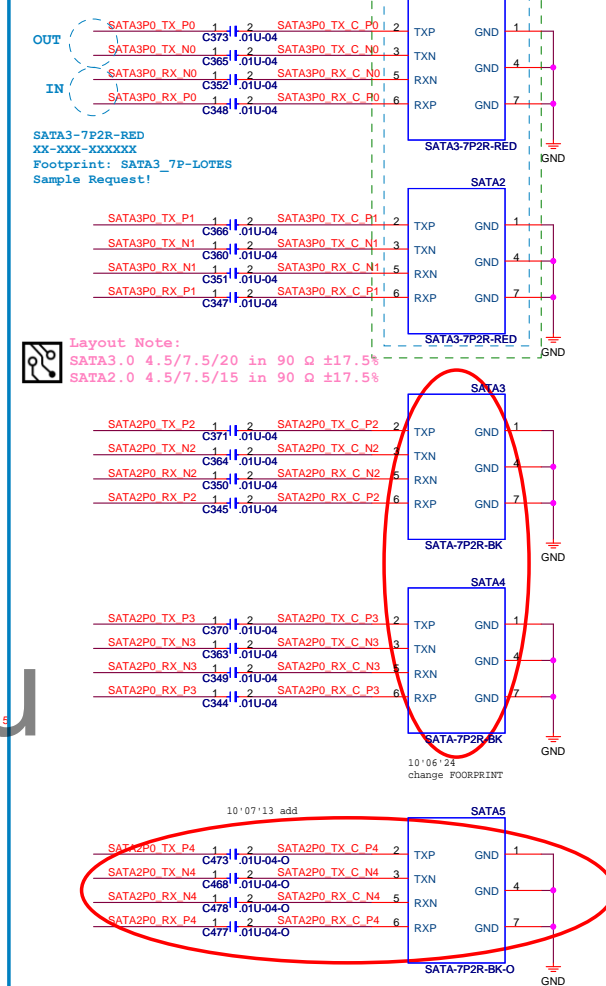
PCH1C
CL_CLK1 BA50
CL_DATA1 BF50
CL_RST1# BF49
PCH MEPWROK R BC46
APWROK
BN21 PWM0
BT21 PWM1
BM20 PWM2
BN19 PWM3
TACH0_GPIO17
TACH1_GPIO1
TACH2_GPIO6
TACH3_GPIO7
TACH4_GPIO68
TACH5_GPIO69
TACH6_GPIO70
TACH7_GPIO71
SST
SCLOCK_GPIO22
SLOAD_GPIO38
SDATAOUT0_GPIO39
SDATAOUT1_GPIO48
U1CPT

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.

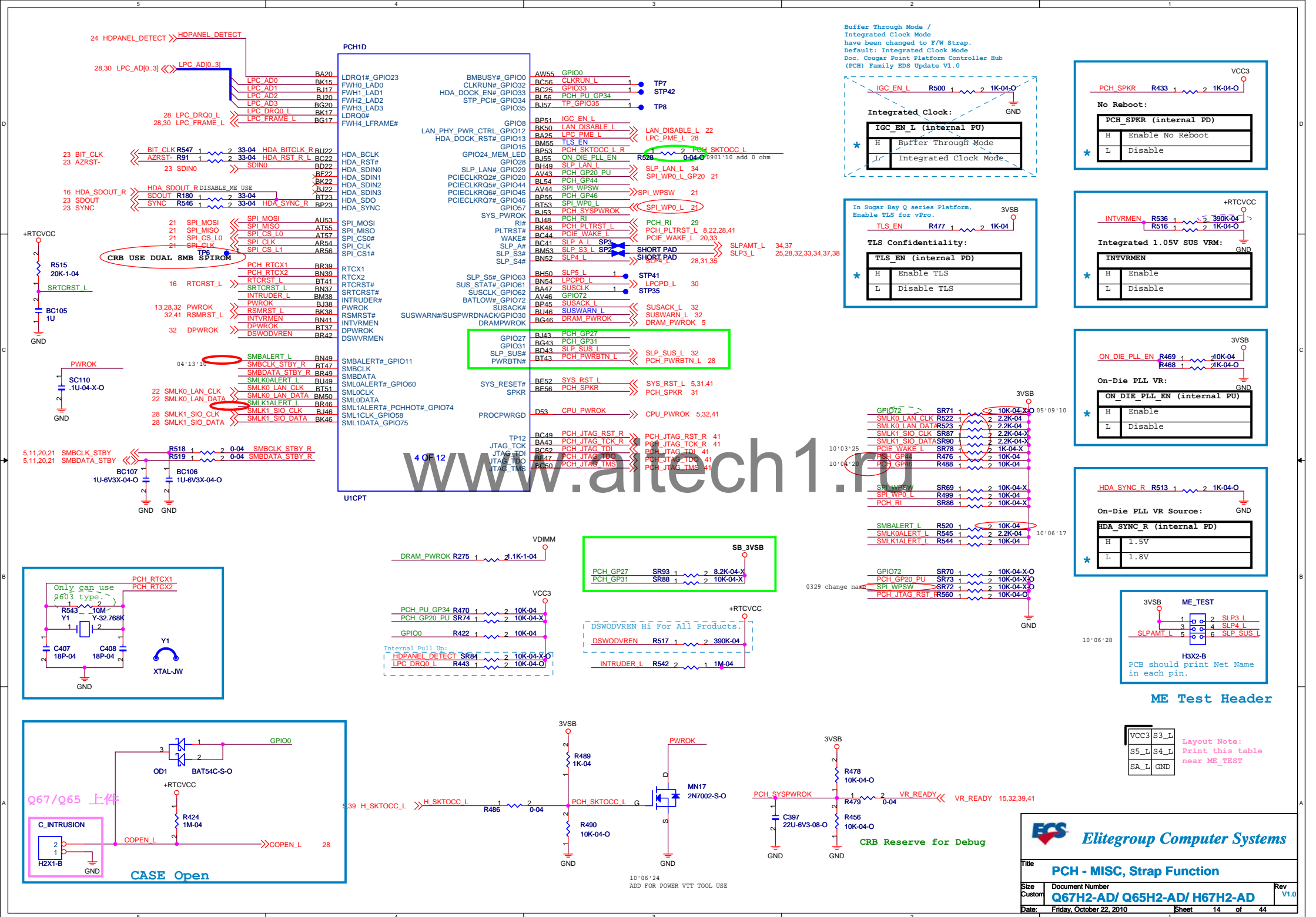
SATA0RXN AC56 SATA3P0 RX N0
SATA0RXP AB55 SATA3P0 RX P0
SATA0TXN AE46 SATA3P0 TX N0
SATA0TXP AE44 SATA3P0 TX P0
SATA1RXN AA53 SATA3P0 RX N1
SATA1RXP AA56 SATA3P0 RX P1
SATA1TXN AG49 SATA3P0 TX N1
SATA1TXP AG47 SATA3P0 TX P1
SATA2RXN AL50 SATA2P0 RX N2
SATA2RXP AL49 SATA2P0 RX P2
SATA2TXN AL56 SATA2P0 TX N2
SATA2TXP AL53 SATA2P0 TX P2
SATA3RXN AN46 SATA2P0 RX N3
SATA3RXP AN44 SATA2P0 RX P3
SATA3TXN AN56 SATA2P0 TX N3
SATA3TXP AN55 SATA2P0 TX P3
SATA4RXN AN49 SATA2P0 RX N4
SATA4RXP AN50 SATA2P0 RX P4
SATA4TXN AT50 SATA2P0 TX N4
SATA4TXP AT49 SATA2P0 TX P4
SATA5RXN AT46 SATA2P0 RX N5
SATA5RXP AT44 SATA2P0 RX P5
SATA5TXN AV50 SATA2P0 TX N5
SATA5TXP AV49 SATA2P0 TX P5
CLKIN_SATA_N AF55 CKG SATA N
CLKIN_SATA_P AG56 CKG SATA P
SATALEDN RF57 SATALED_L
SATAICOMP1 AJ55 SATA1RCOMP R409
SATAICOMP2 BC54 GPIO21
SATA1GP_GPIO19 AY52 GPIO19
SATA2GP_GPIO36 BB55 GPIO36
SATA3GP_GPIO37 BG53 GPIO37
SATA4GP_GPIO16 AL56 GPIO16
SATA5GP_GPIO49 BA56 GPIO49
SATA3COMP1 AE54 SATA3RCOMP R405
SATA3COMP2 AE52 PCH TP16
TP16 STP32
SATA3RBIAS AC52 SATA3RBIAS SR68
A20GATE INTR3_3V_B BN55 INTR3_3V_B
KB_RST_L 28 KB_RST_L 28
SER_IRQ 28 SER_IRQ 28
PMSYNCH F55 PM_SYNC STP26 SHORT PAD CPU_THERMTRIP_L 5

PECI SIGNAL, CRB RESERVE CONNECT FROM CPU

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.



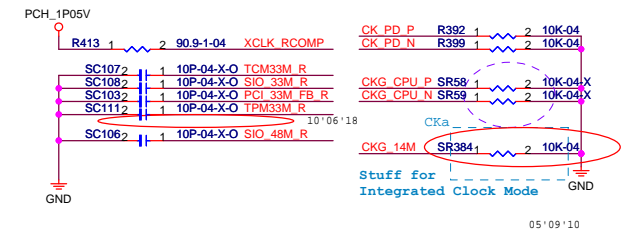
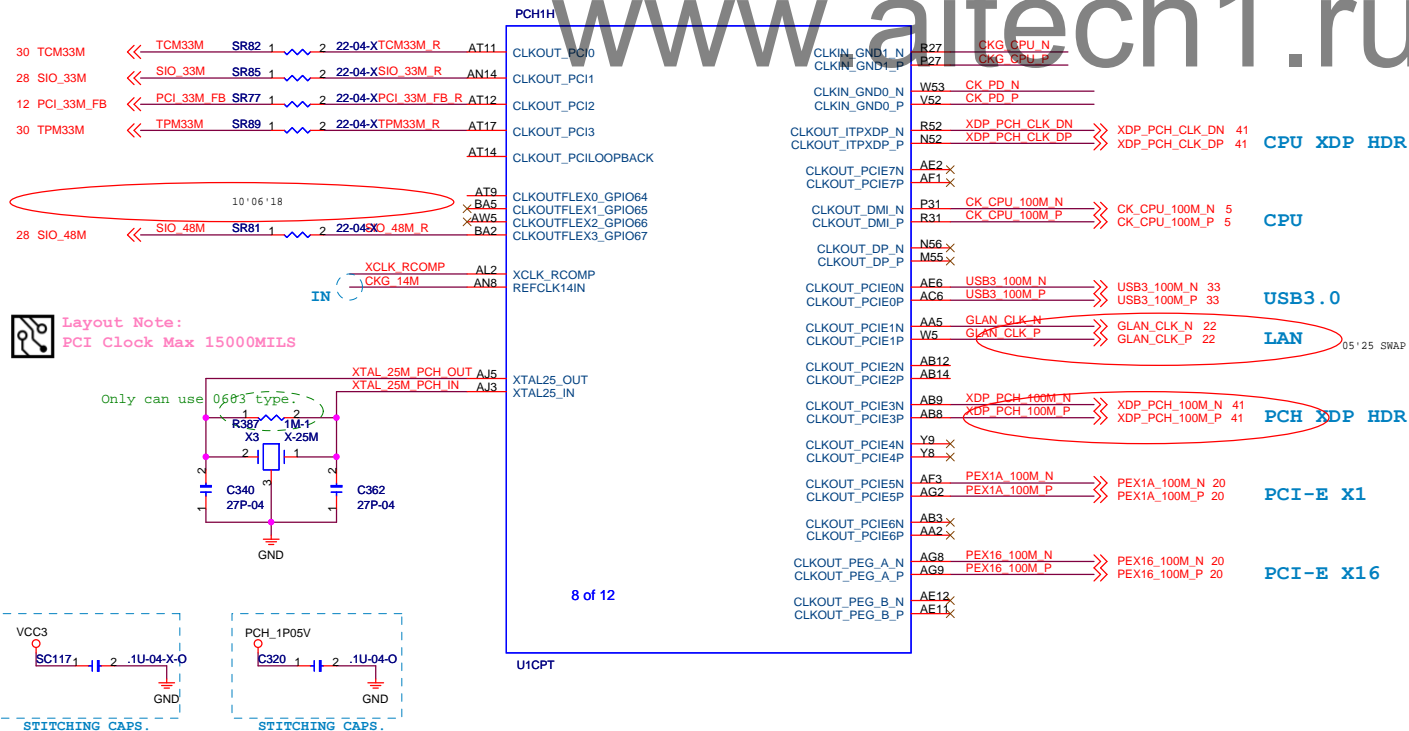
INTERNAL SATA CONNECTOR



0908'10 TAKE OFF CLK GEN

CLK GEN.Seligo SLG421 Circuit.

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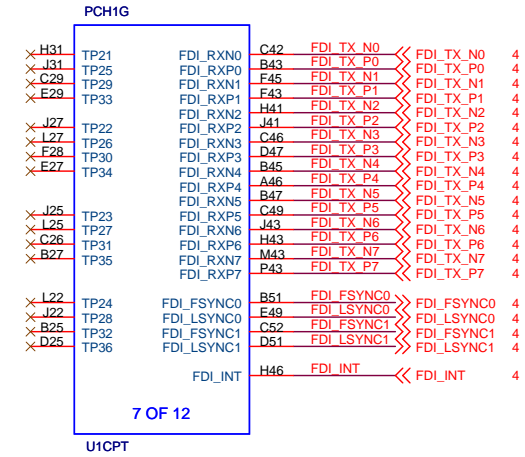
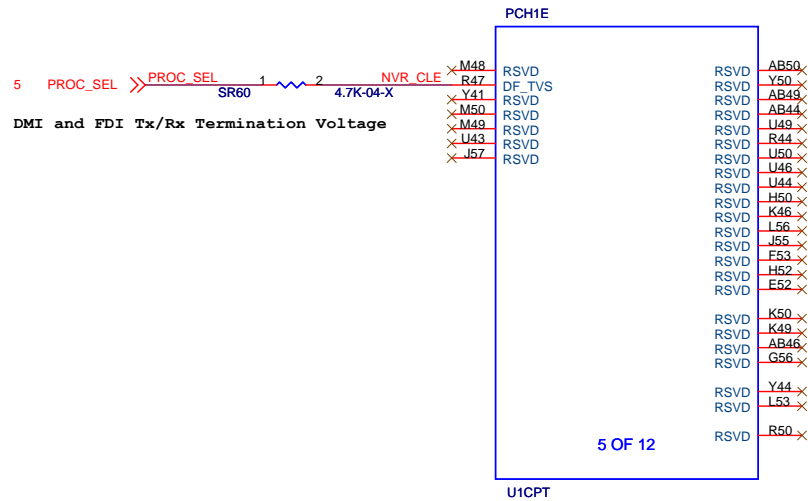


10'03'24

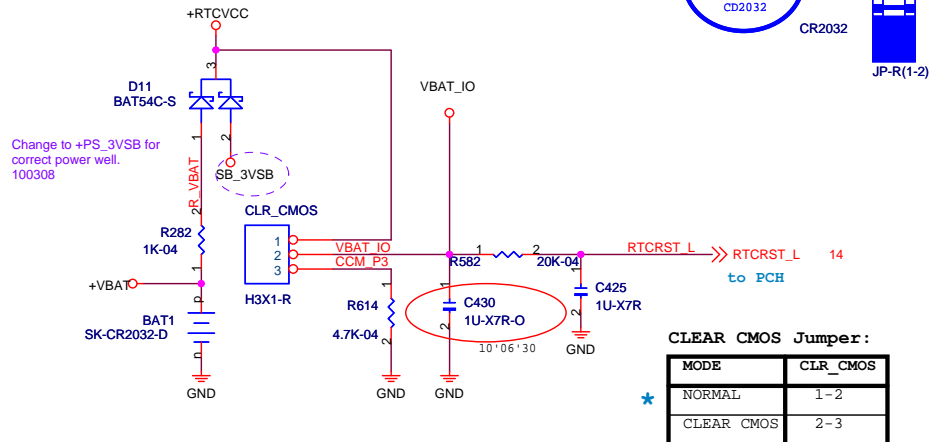
Clock Mode	CLK GEN. Seligo SLG421 Circuit.	CKa
Integrated Clock Mode	x	v
Buffer Through Mode	y	x

Elitegroup Computer Systems

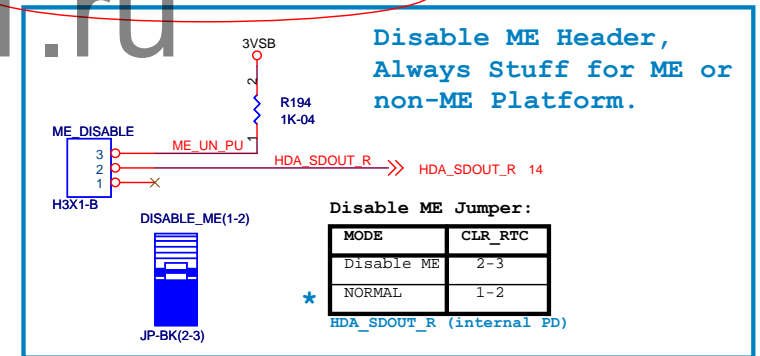
Title		
PCH - CLK IO, CKG - SLG421		
Size	Document Number	Rev
Custom	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0
Date:	Friday, October 22, 2010	Sheet 15 of 44



CLR_CMOS



04'20'10 CHANGE JUMPER DEFINE



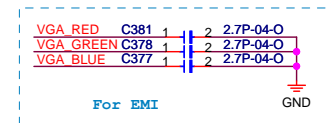
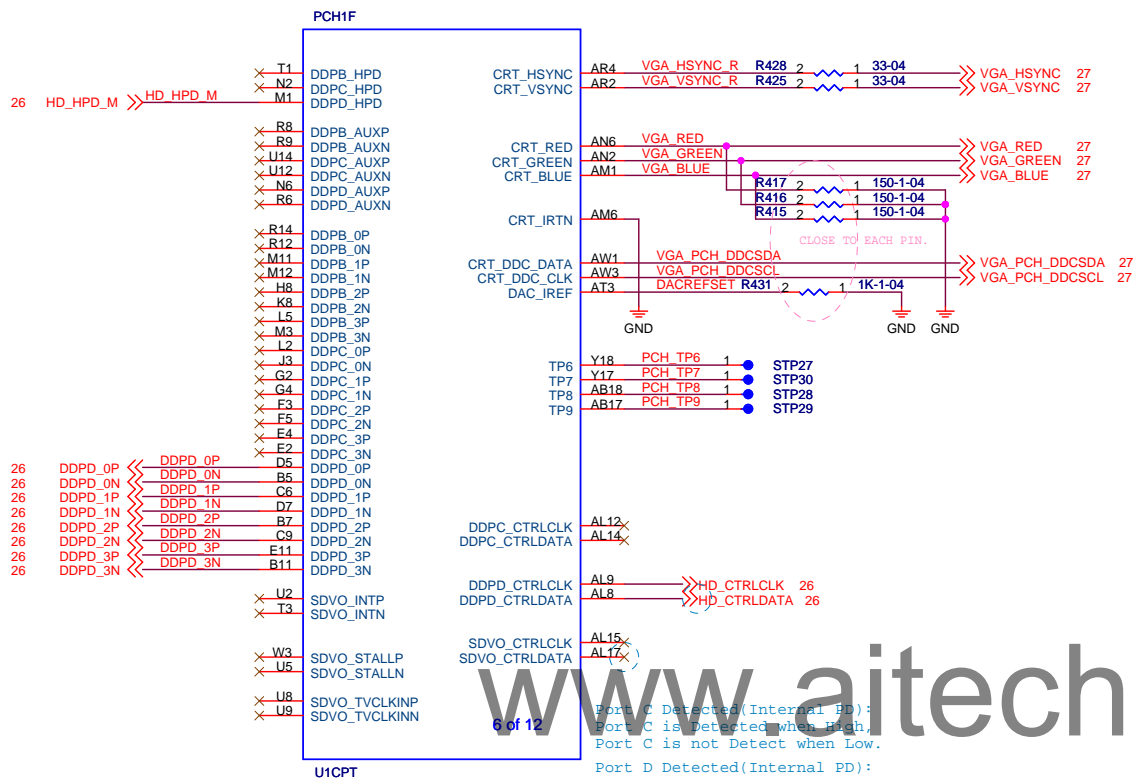
ECS Elitegroup Computer Systems

Title **PCH - NVRAM/FDI, CLR_CMOS**

Size B Document Number **Q67H2-AD/ Q65H2-AD/ H67H2-AD** Rev V1.0

Date: Friday, October 22, 2010 Sheet 16 of 44

Port-D:
DVI



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6 of 12

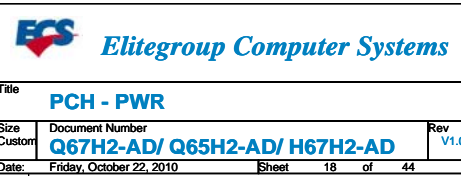
Port C Detected (Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.

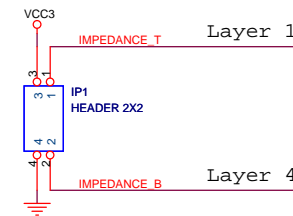
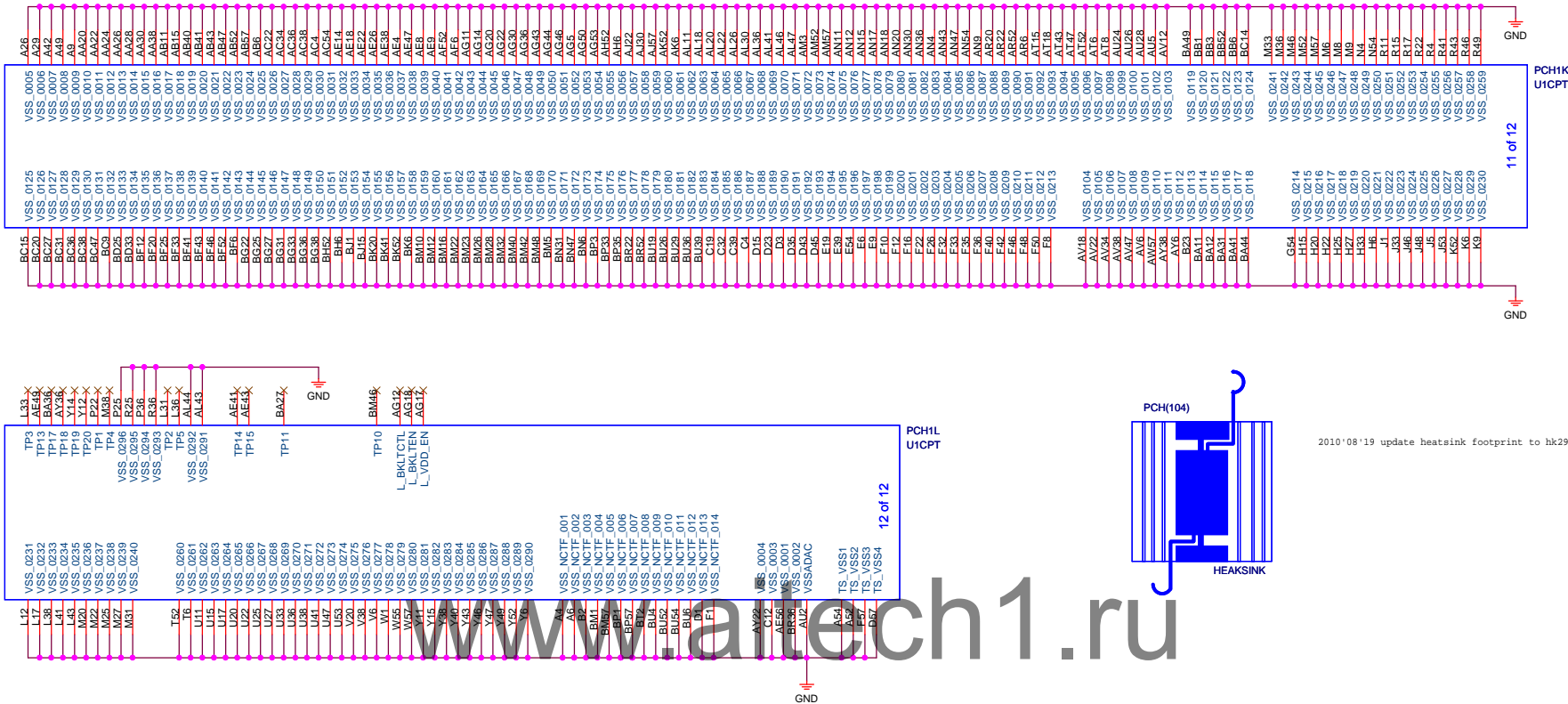
Port D Detected (Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.

Port B Detected (Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.

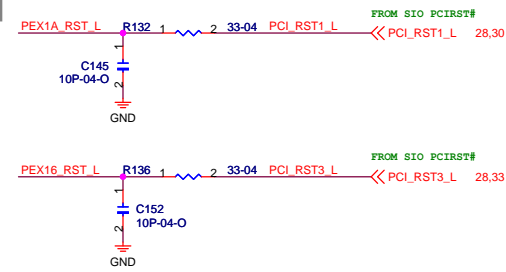
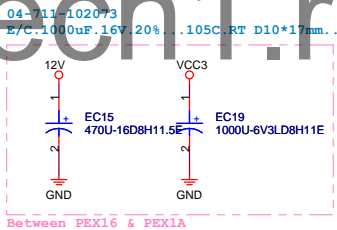
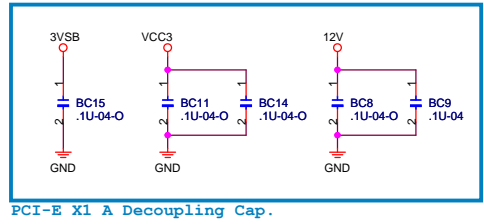
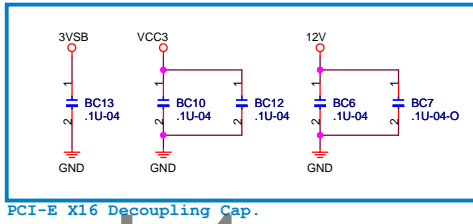
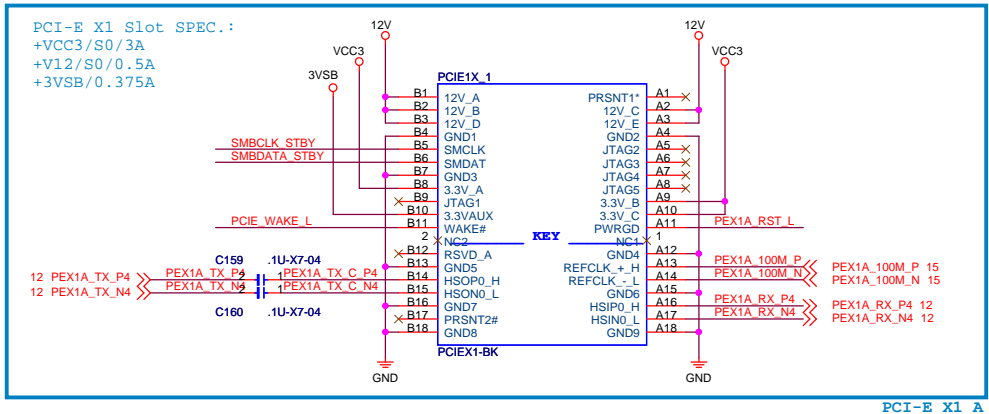
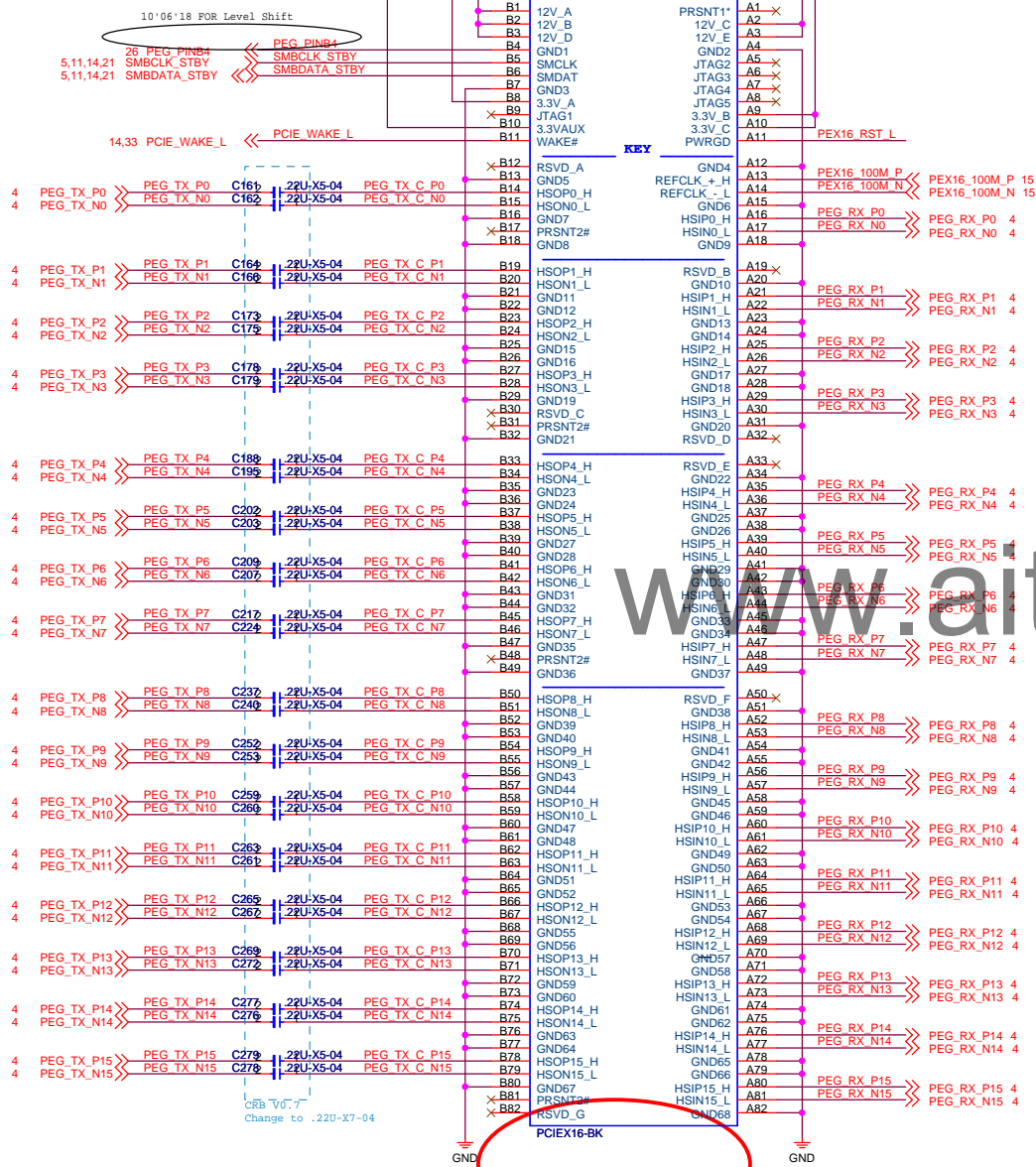


Title		
PCH - DP/VGA		
Size	Document Number	Rev
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Date:	Friday, October 22, 2010	Sheet 17 of 44

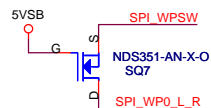
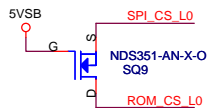
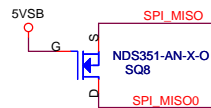
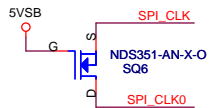
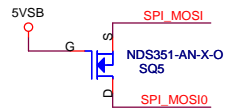
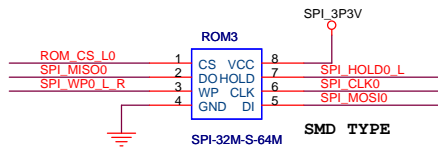
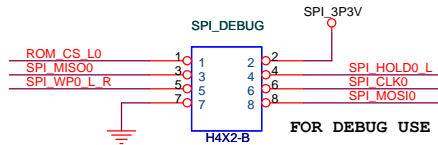
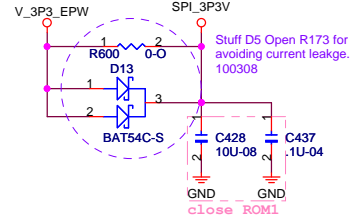
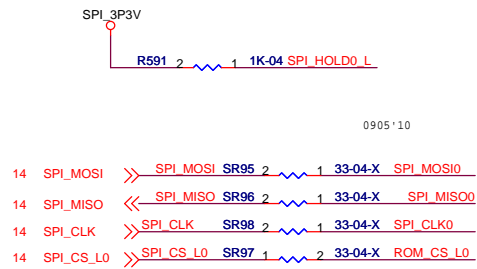




PCI-E X16 Slot SPEC.:
 +VCC3/S0/3A
 +V12/S0/5.5A
 +3VSB/0.375A



SPI ROM Circuit



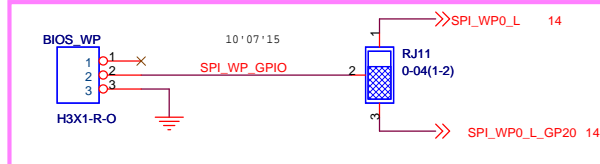
03-080-535136 MOSFET N-CH.NDS351AN-NL..Vds=-30V,Vgs=20V.Id=1.4A...SOT-23.Rds(on)=160mOHM.
LEAD-FREE,FAIRCHILD
(替)03-050-540682

BIOS_WP(1-2)



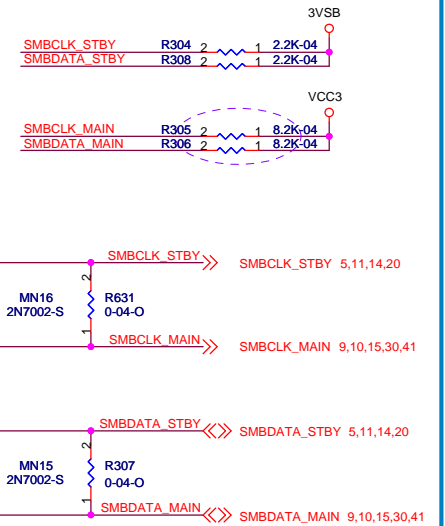
BIOS WP Jumper:

MODE	CLR_CMOS
BIOS WP	1-2
NORMAL	2-3



Q67/Q65 上件

SMBUS Logic Circuit

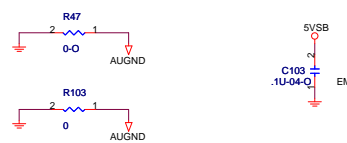
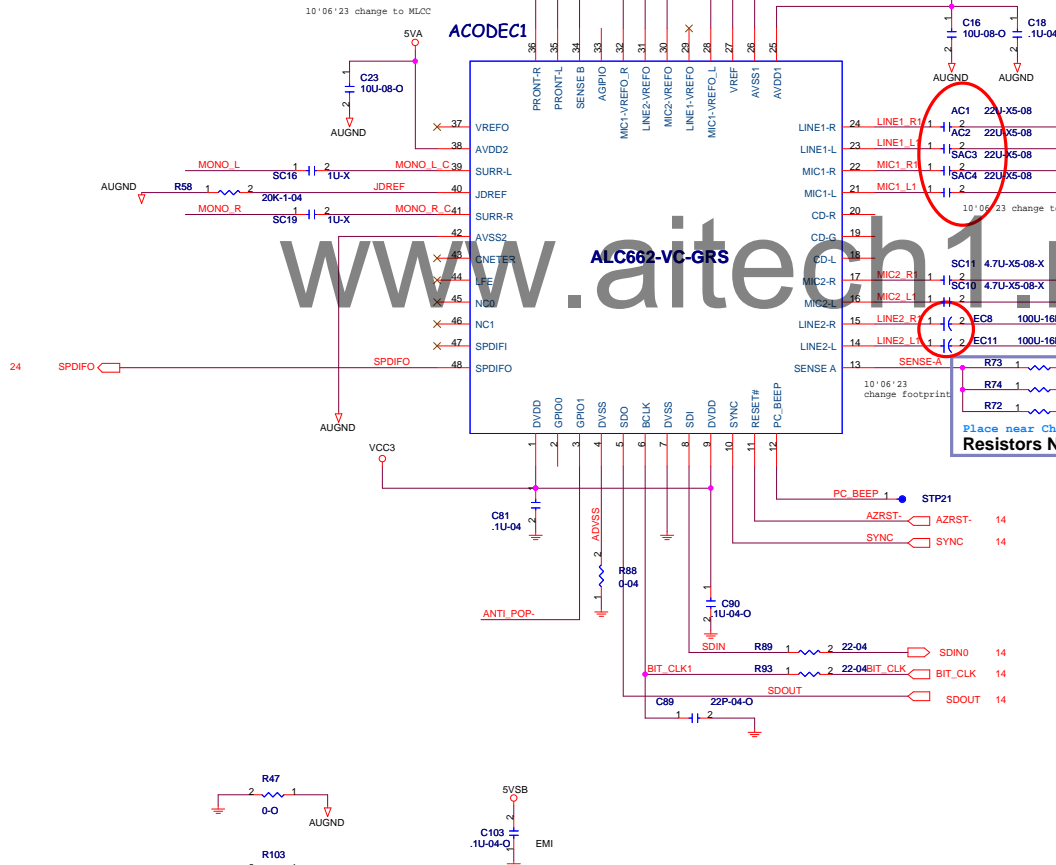
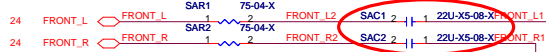
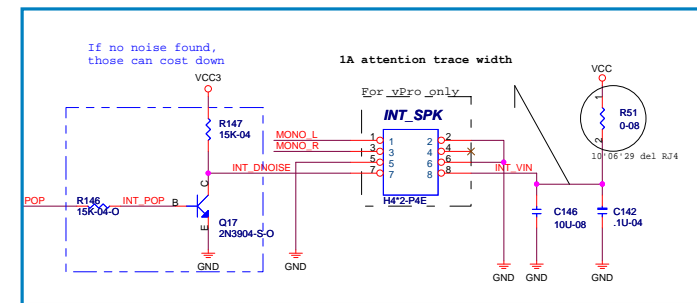
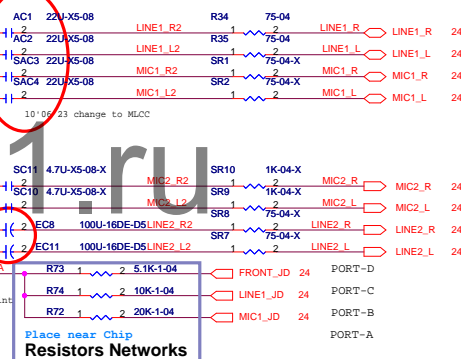
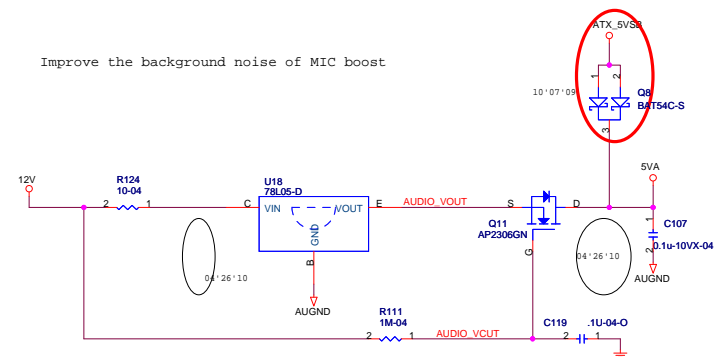
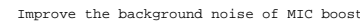


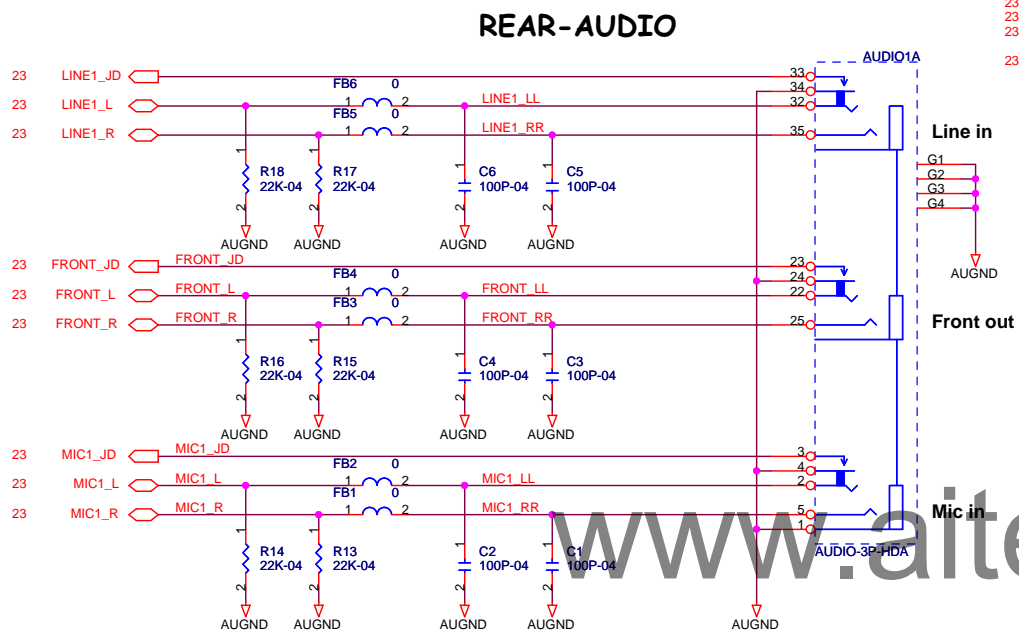
Layout Note:
SMBUS Trace Max 21500MILS

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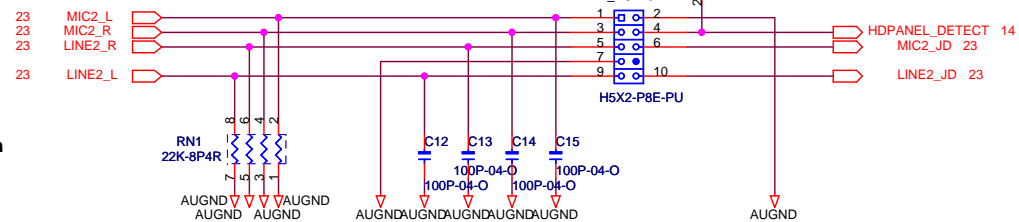
Depop schematic

The schematic diagram illustrates the 'Depop' stage of a circuit. It features several 2N3906-S transistors (Q13, Q14, Q12, Q16) and various passive components. Key components include a 10K-04 resistor (R84) connected to VCC3, a 22u-250C capacitor (EC25), and a 220K-04 resistor (R140) connected to 3VSB. The circuit also includes a Zener diode (AZRST) and several other resistors (R90, R67, R143). The signal path is indicated by red lines, showing the flow from the input through the transistor stages to the output (POP).

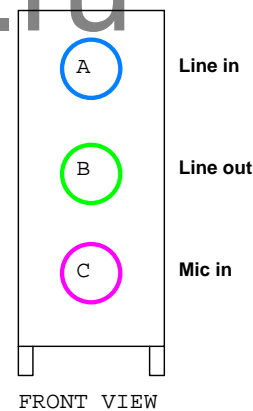
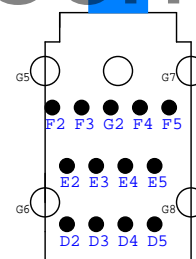
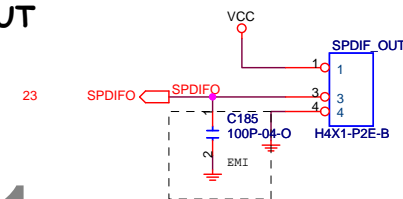
[illegible]



FRONT-AUDIO

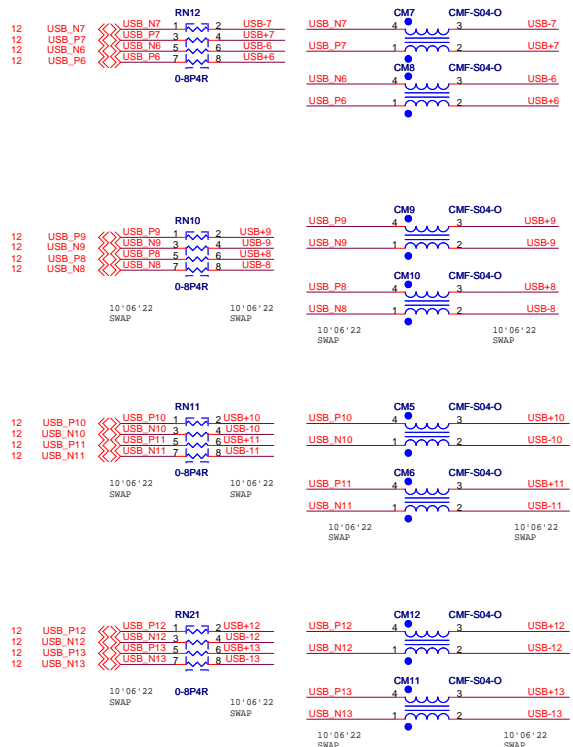


SPDIF-OUT



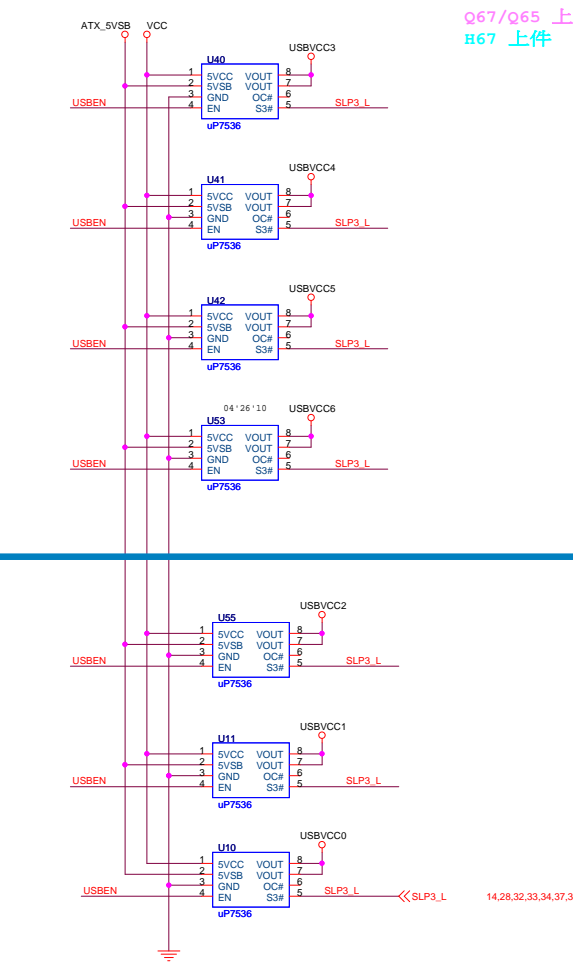
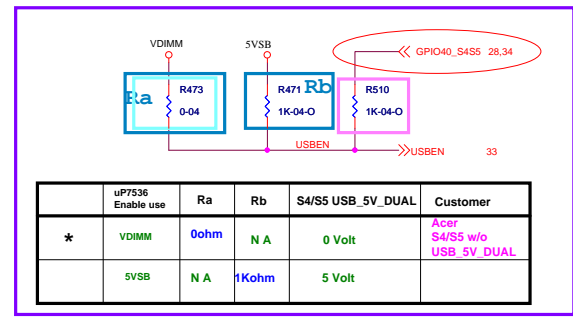
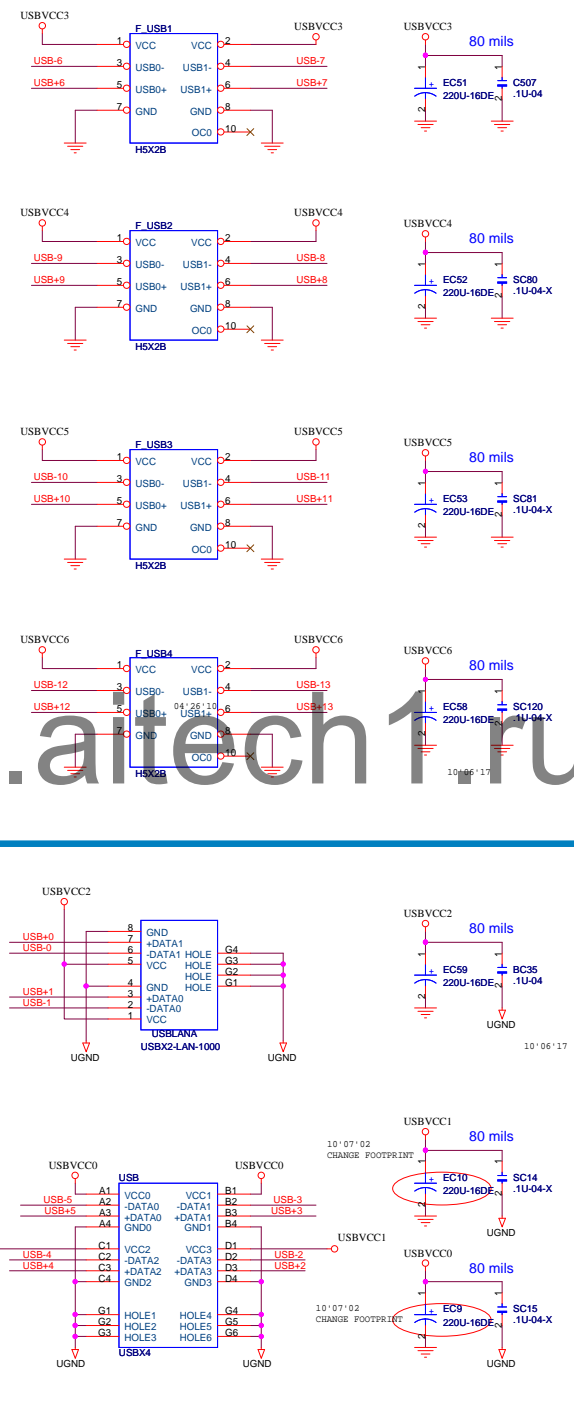
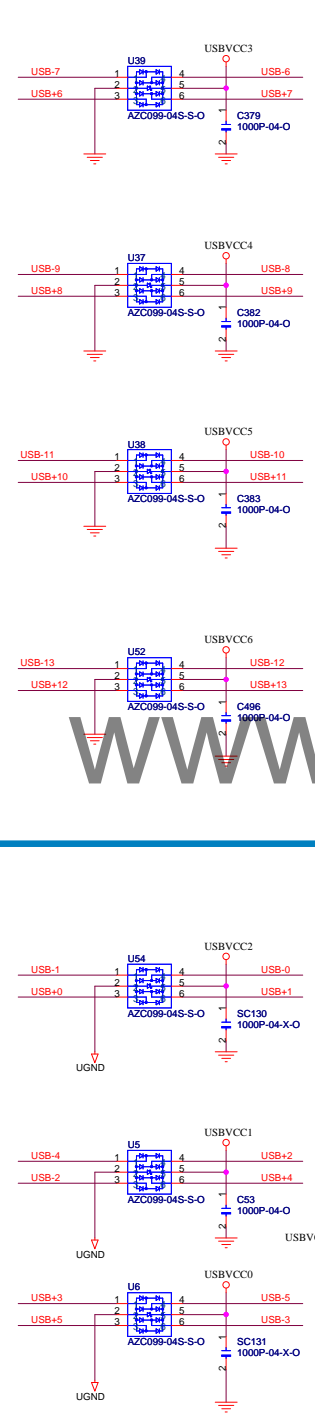
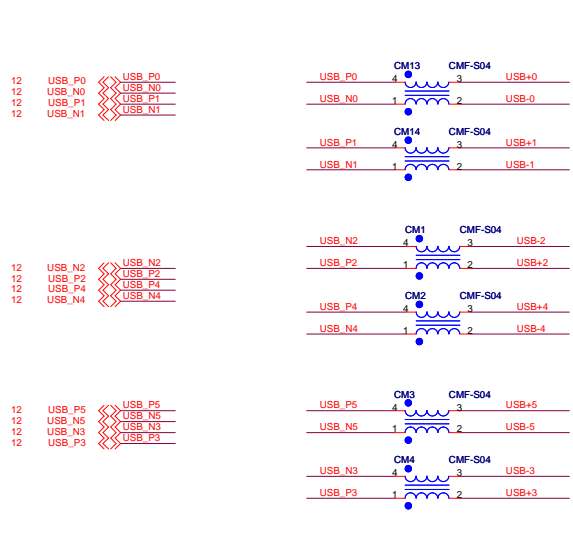
Elitegroup Computer Systems

Title		
AUDIO ALC662 (PANEL)		
Size	Document Number	Rev
B	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0
Date:	Friday, October 22, 2010	Sheet 24 of 44



FRONT PANEL USB HEADER

REAR PANEL USB HEADER



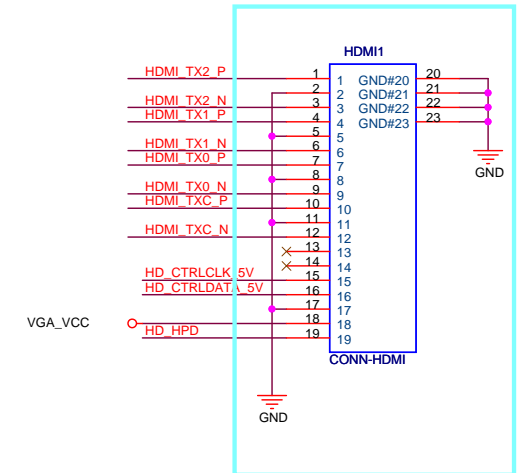
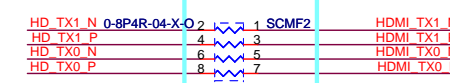
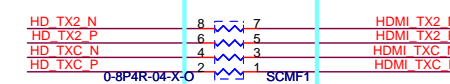
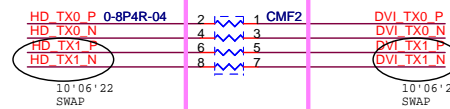
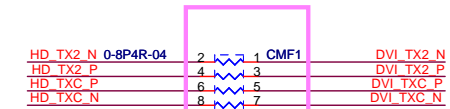
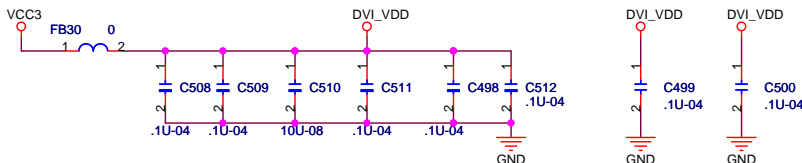
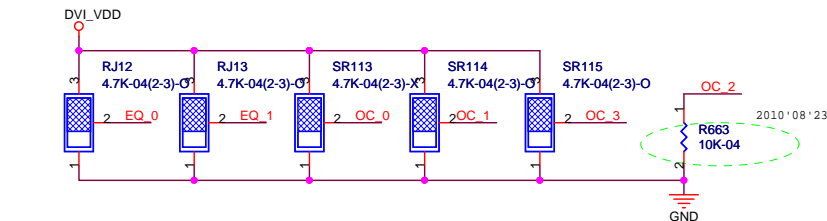
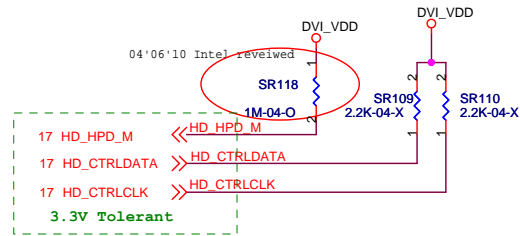
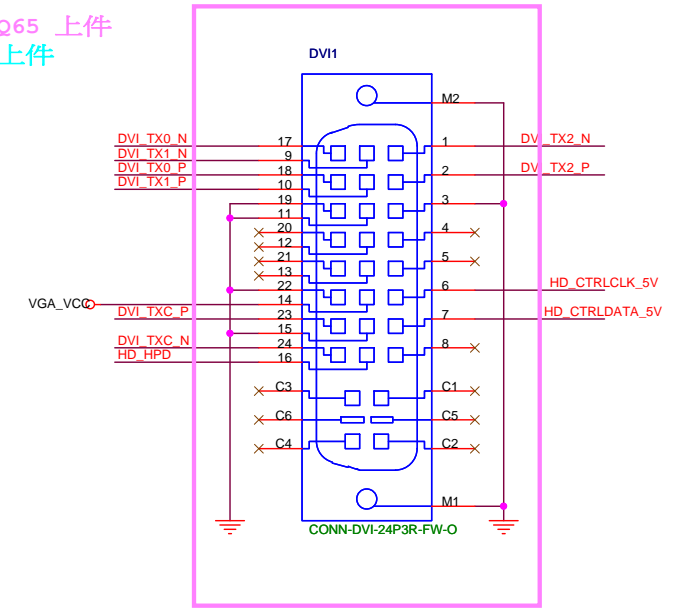
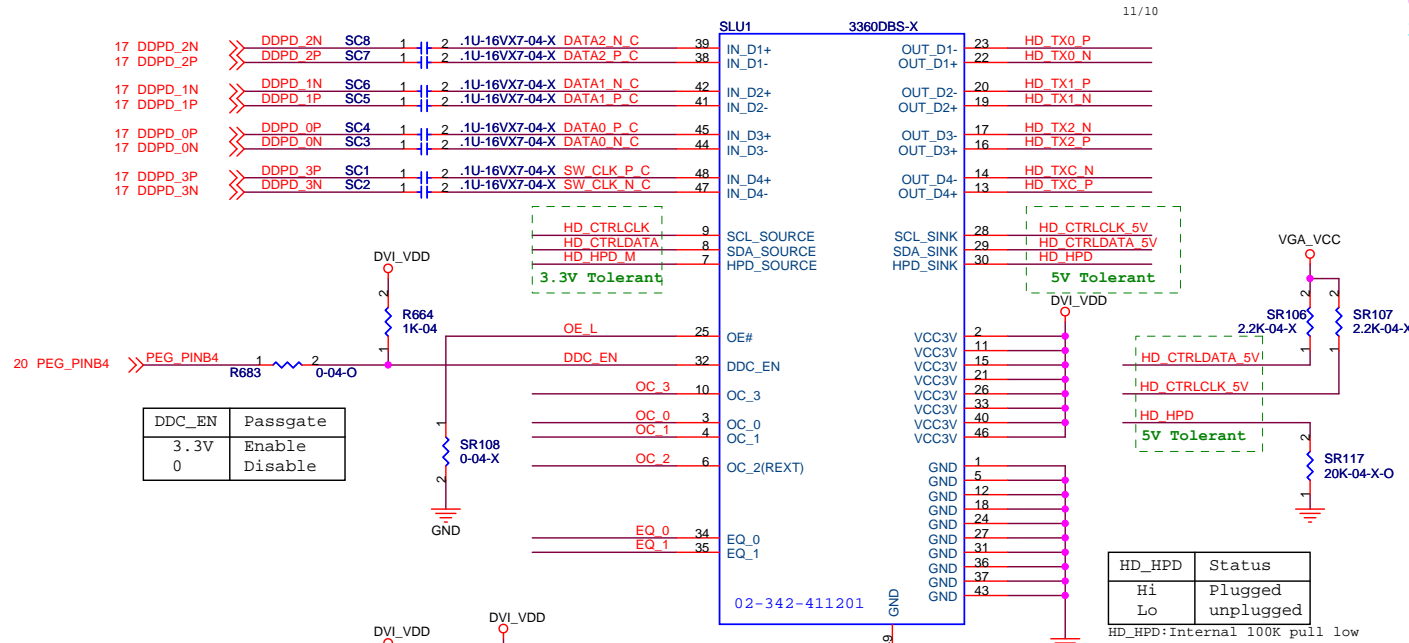
Elitegroup Computer Systems

Title: **USB - PWR/CONN/HDR**

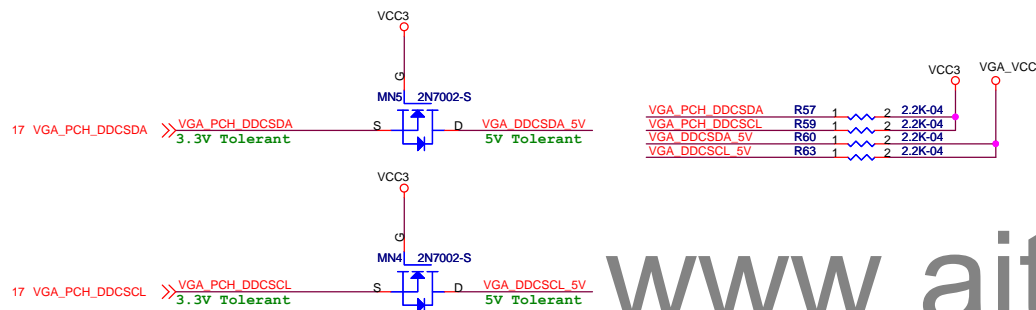
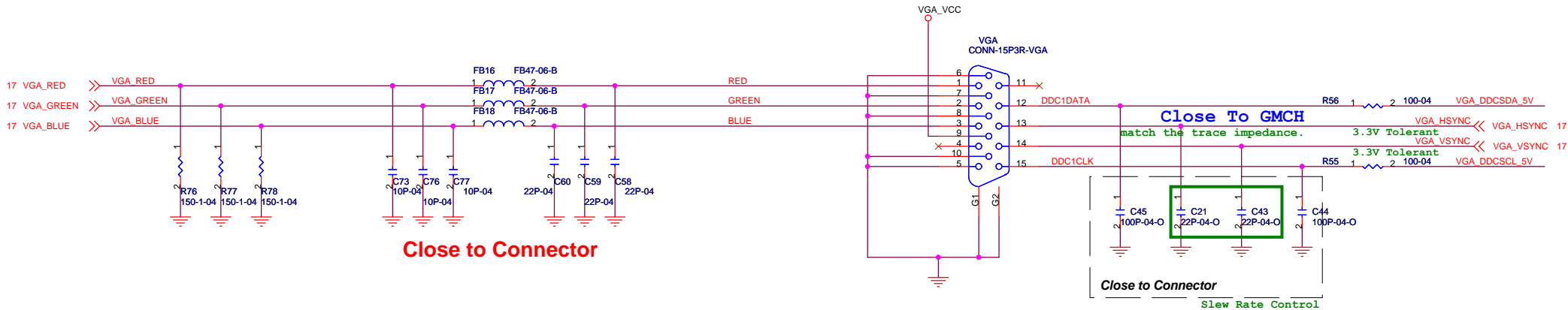
Size Custom: Document Number: **Q67H2-AD/ Q65H2-AD/ H67H2-AD** Rev V1.0

Date: Friday, October 22, 2010 Sheet 25 of 44

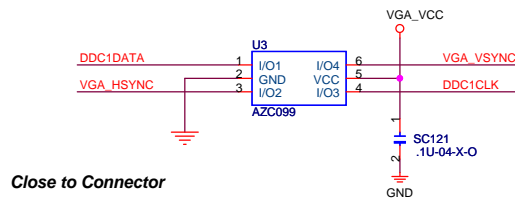
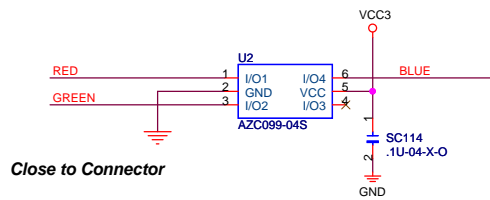
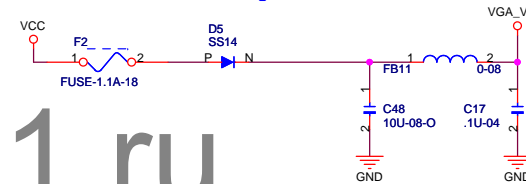
Level Shifter



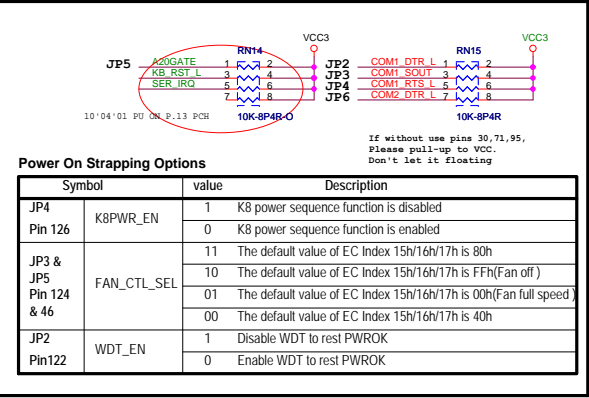
Elite  Computer Systems

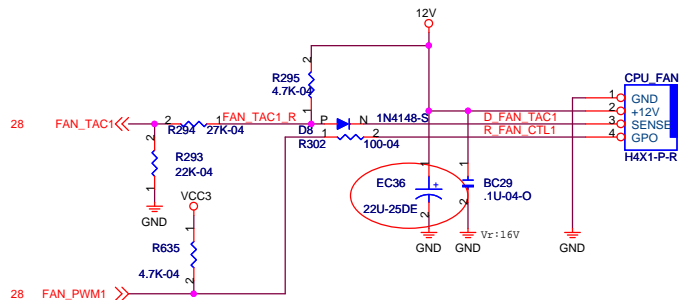


If build in Internal DVI/HDMI Con,
that can use the circuit to protect reverse voltage together.

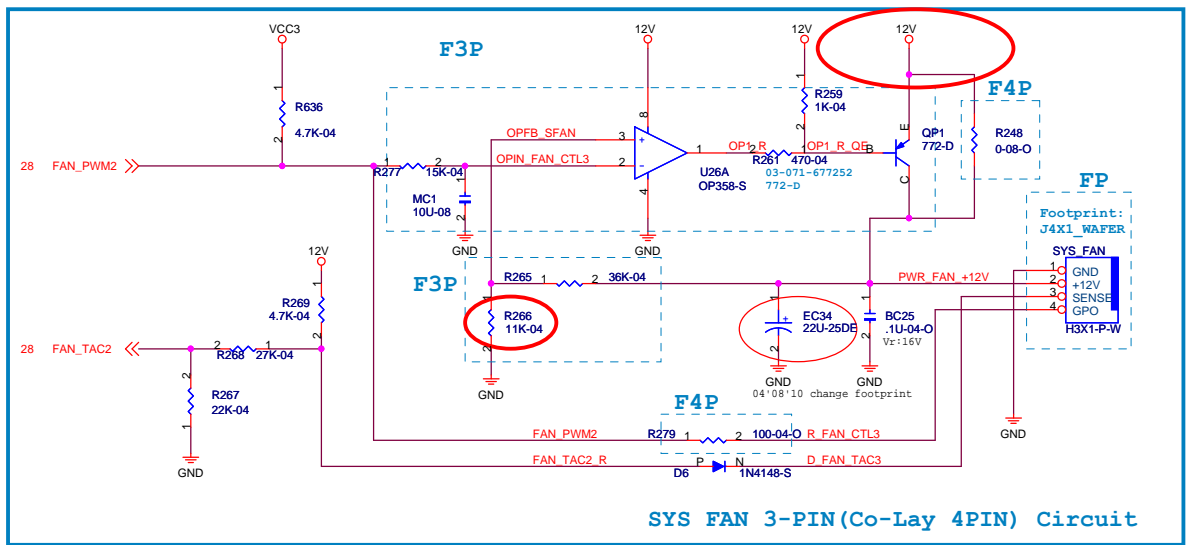


Elitegroup Computer Systems			
Title			
VGA CONNECTOR			
Size	Document Number	Rev	
Custom	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0	
Date:	Friday, October 22, 2010	Sheet	27 of 44



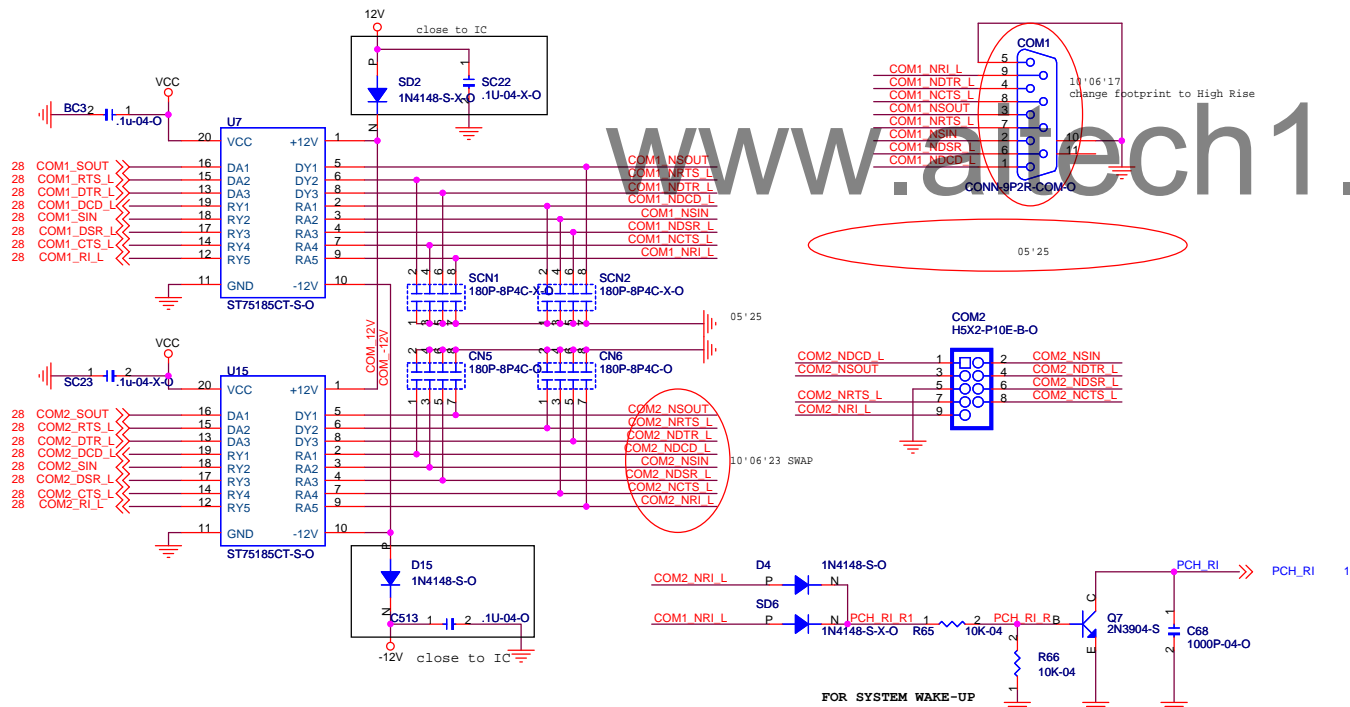


CPU FAN 4-PIN Circuit



SYS FAN 3-PIN (Co-Lay 4PIN) Circuit

COM PORT I/O



Q67/Q65 上件

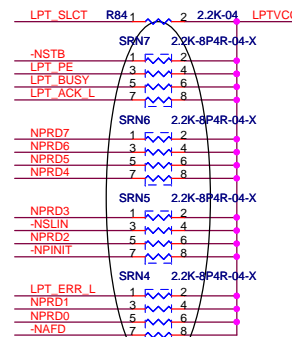
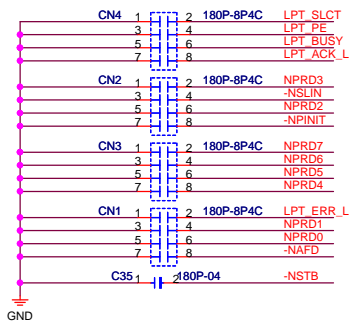
PWR FAN:

MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

28 LPT_D[7..0] >> LPT_D[7..0]
 28 LPT_STB_L >> LPT_STB_L
 28 LPT_ACK_L >> LPT_ACK_L
 28 LPT_BUSY >> LPT_BUSY
 28 LPT_PE >> LPT_PE
 28 LPT_SLCT >> LPT_SLCT
 28 LPT_AFD_L >> LPT_AFD_L
 28 LPT_ERR_L >> LPT_ERR_L
 28 LPT_INIT_L >> LPT_INIT_L
 28 LPT_SLIN_L >> LPT_SLIN_L

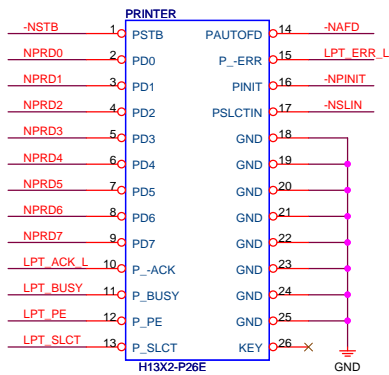
LPT_AFD_RN6 1 2 22-8P4R-04 -NAFD
 LPT_D0 3 4 NPRD0
 LPT_D1 5 6 NPRD1
 LPT_STB_L 7 8 -NSTB
 LPT_D7 7 8 NPRD7
 LPT_D6 7 8 NPRD6
 LPT_D5 7 8 NPRD5
 LPT_D4 7 8 NPRD4
 LPT_INIT_RN7 1 2 22-8P4R-04 -NPINIT
 LPT_D2 3 4 NPRD2
 LPT_SLIN_L 5 6 -NSLIN
 LPT_D3 7 8 NPRD3

10'06'18
 change footprint 8P4R to 8P4R-0402



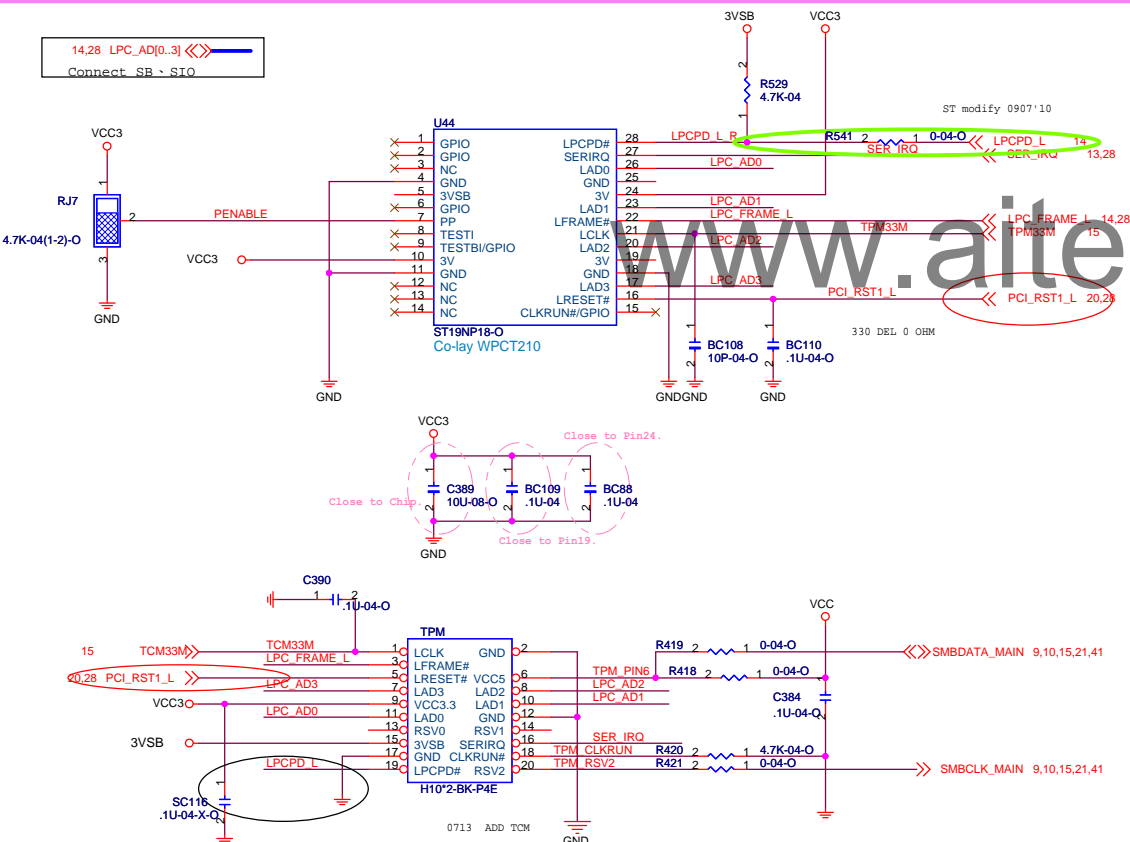
10'06'18
 change footprint 8P4R to 8P4R-0402

Q67/Q65 上件

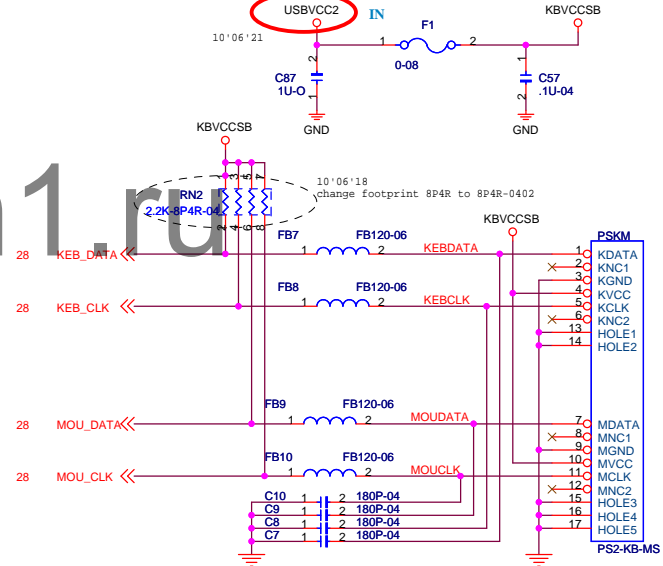


LPT Header Circuit

14,28 LPC_AD[0..3] >> Connect_SB - SIO



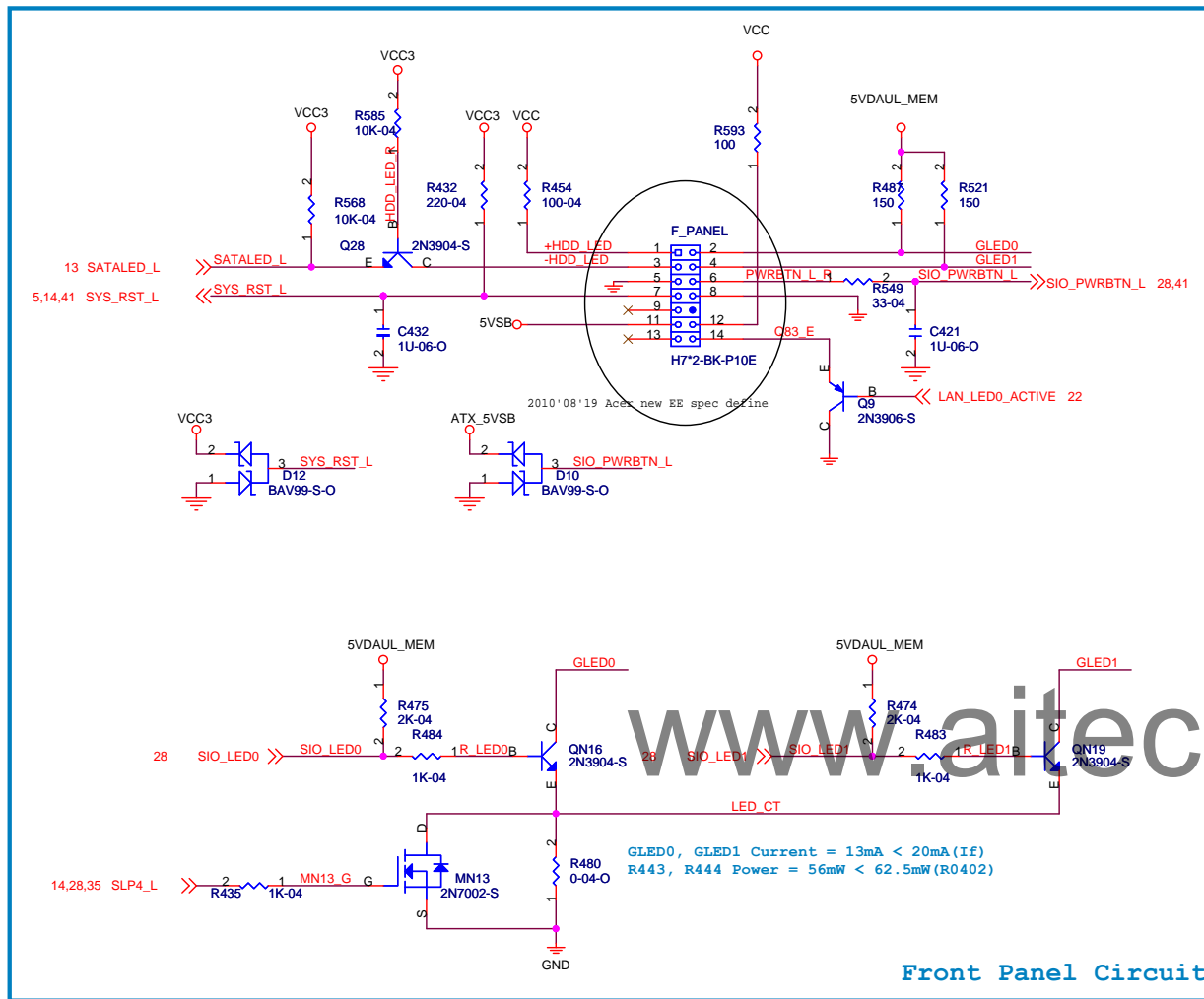
TPM CHIP/Header Circuit



PS2-KB Circuit

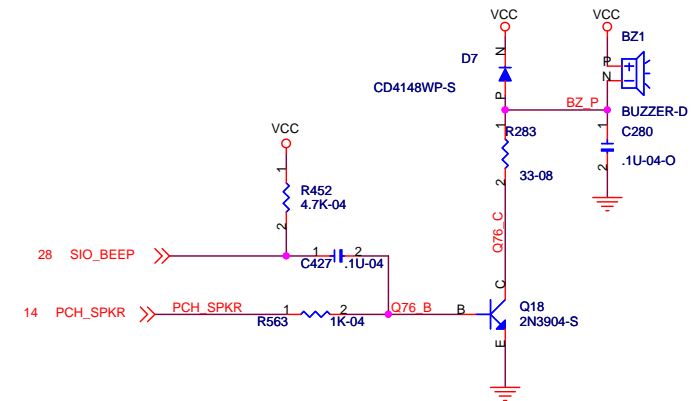
Elitegroup Computer Systems

Title	TPM, PS/2, LPT		
Size	Document Number	Rev	
Custom	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0	
Date:	Friday, October 22, 2010	Sheet	30 of 44



Front Panel Circuit

Buzzer Circuit



Elitegroup Computer Systems

Title

F_PANEL, BUZ

Size

Document Number

Q67H2-AD/ Q65H2-AD/ H67H2-AD

Rev

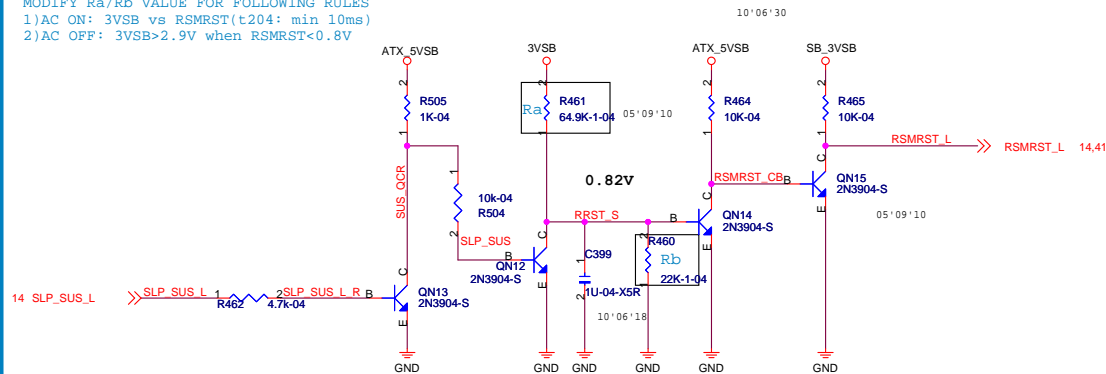
V1.0

Date: Friday, October 22, 2010

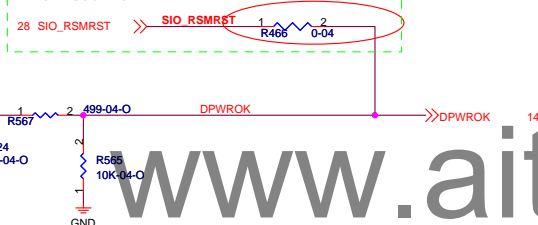
Sheet 31 of 44

MODIFY Ra/Rb VALUE FOR FOLLOWING RULES

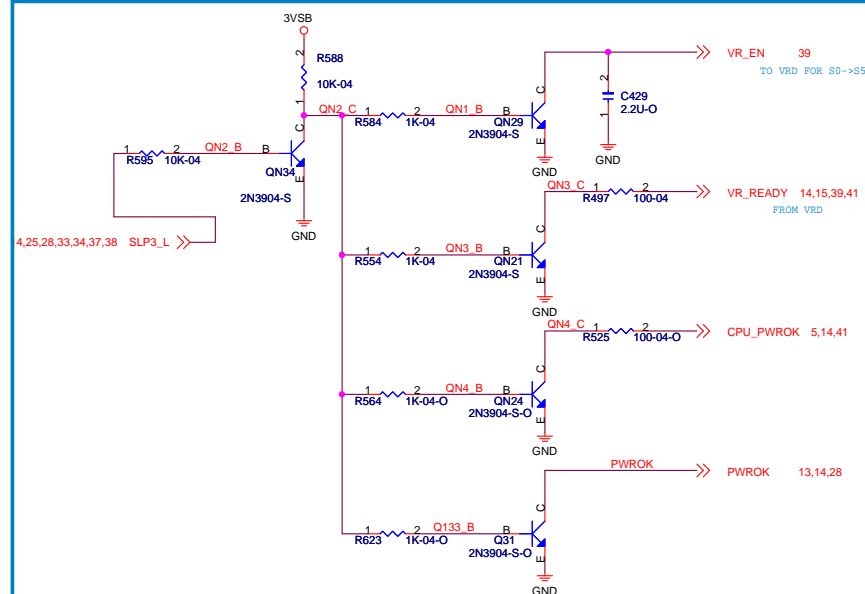
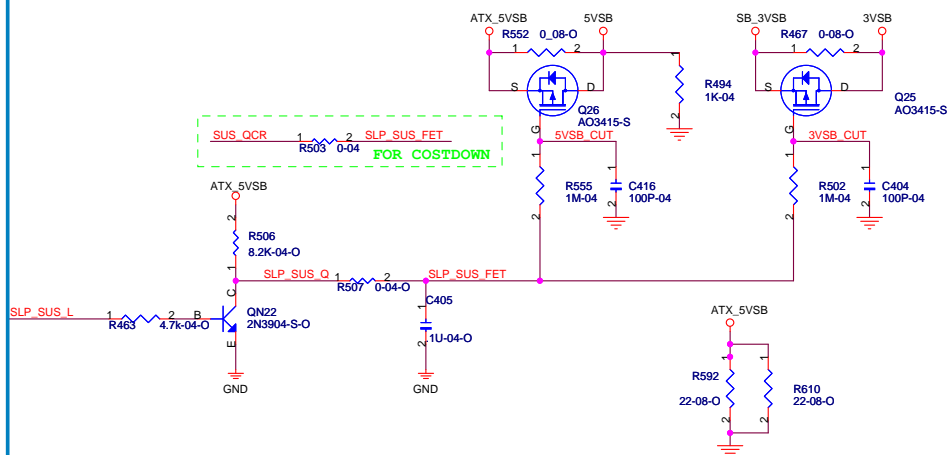
- 1) AC ON: 3VSB vs RSMRST(t204: min 10ms)
- 2) AC OFF: 3VSB>2.9V when RSMRST<0.8V



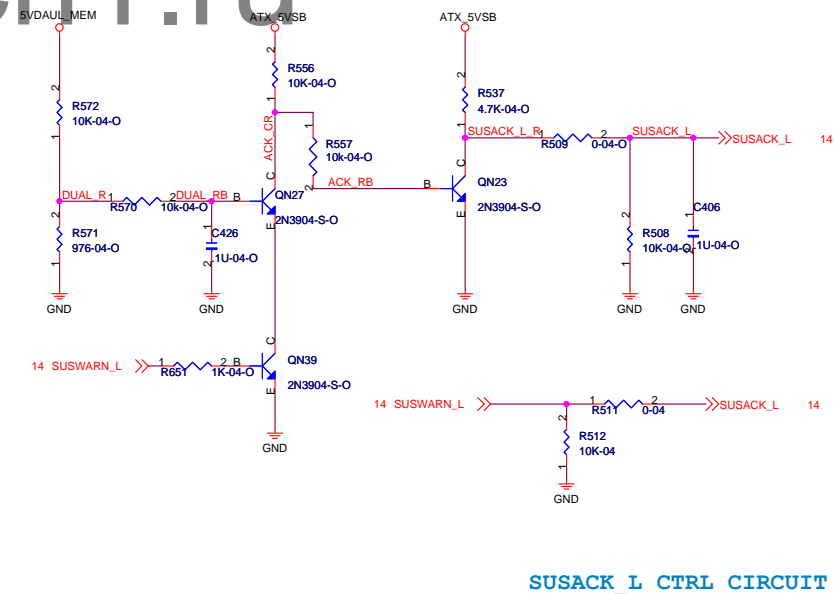
FOR COSTDOWN

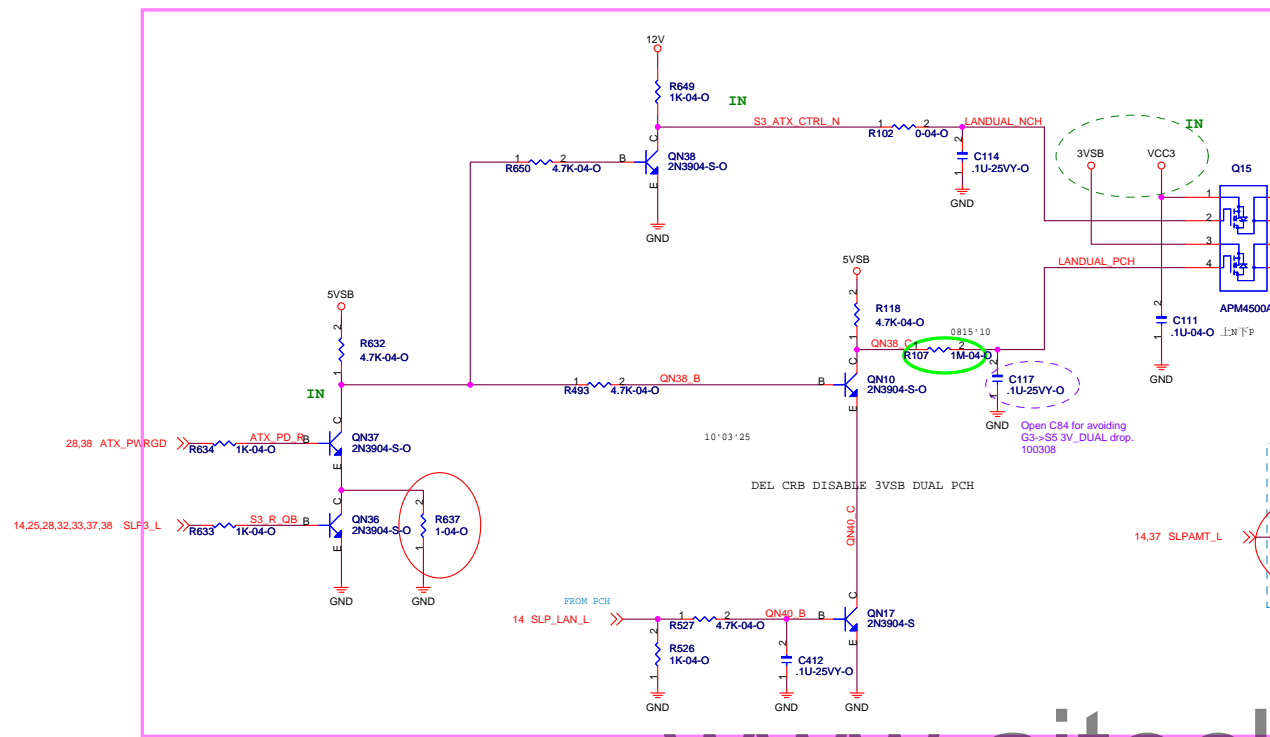


SUS QCR 1 2 SLP SUS FET
R503 0-04
FOR COSTDOWN

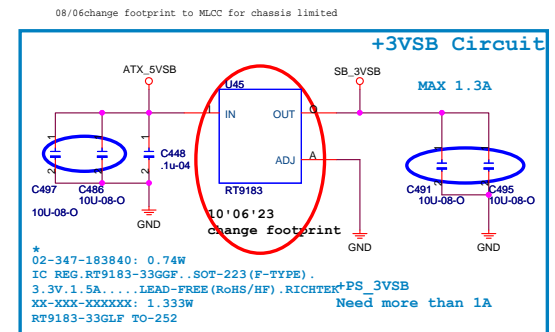
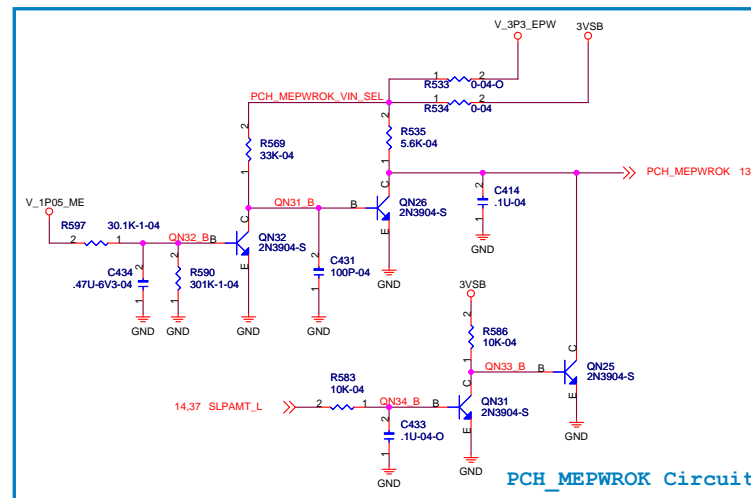
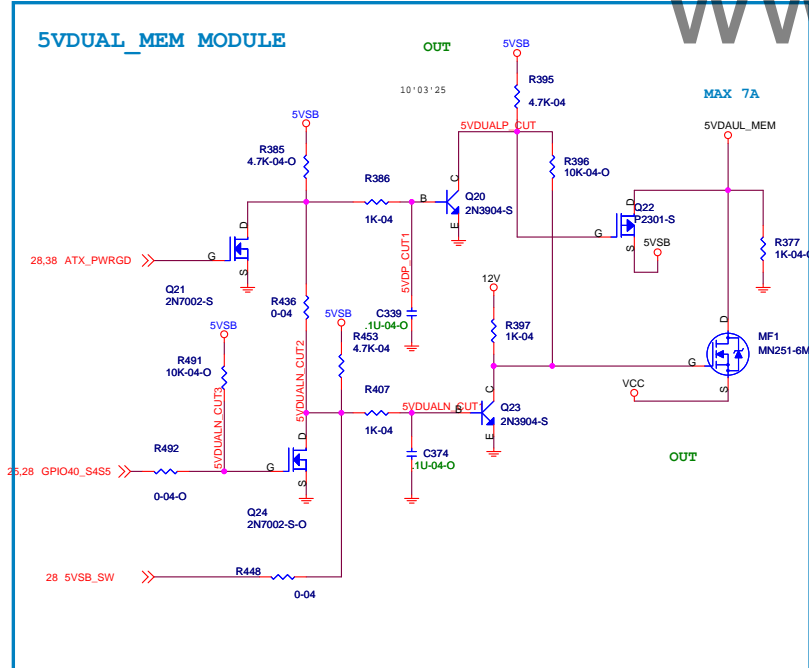
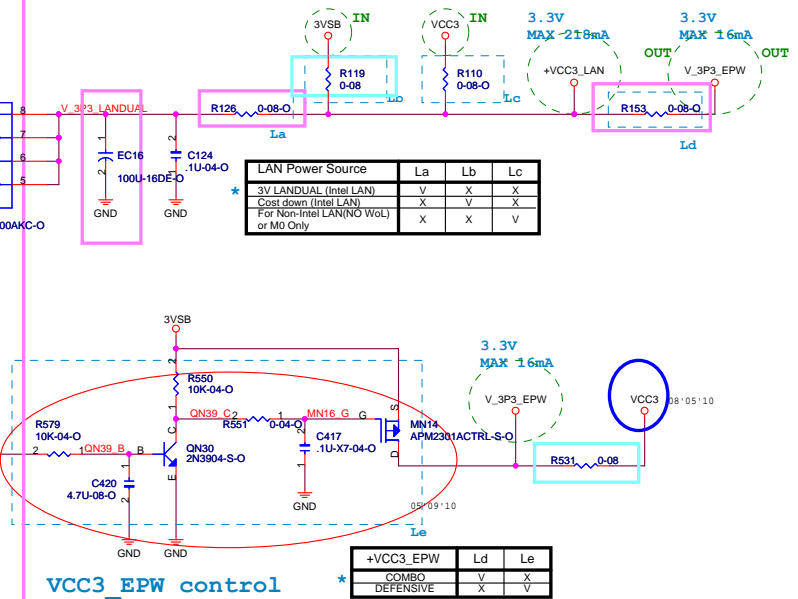


Power Down Sequencing Circuit





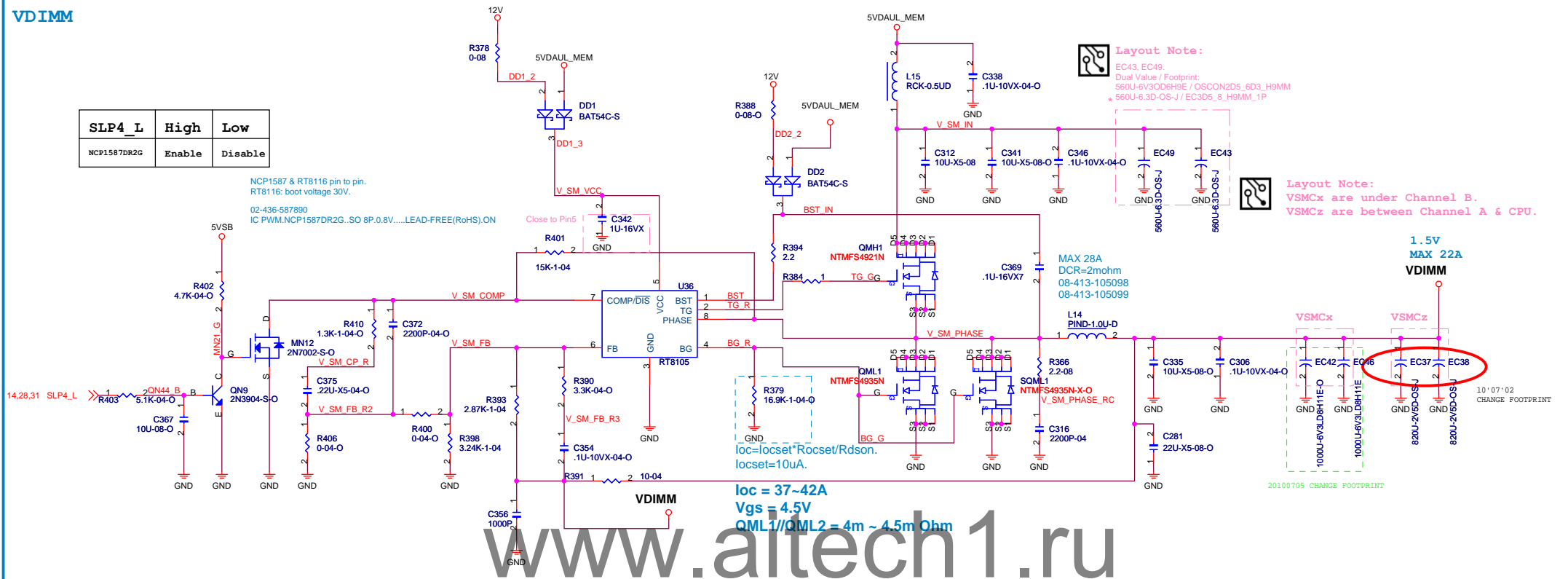
Q67/Q65 上件
H67 上件



VDIMM

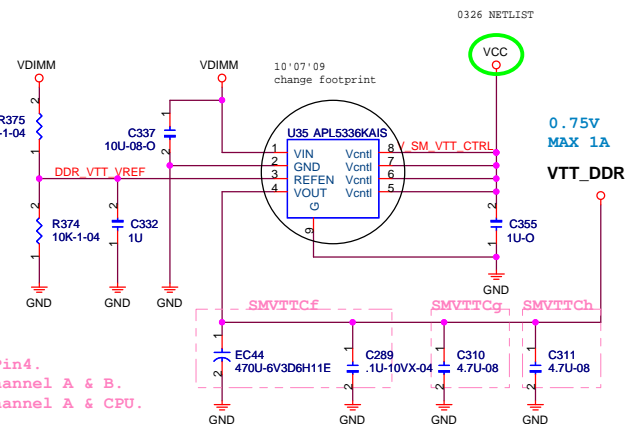
SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.
02-436-587890
IC PWM.NCP1587DR2G..SO 8P.0.8V.....LEAD-FREE(RoHS).ON



DDR_VTT

CRS RESERVE S3 CTRL CKT

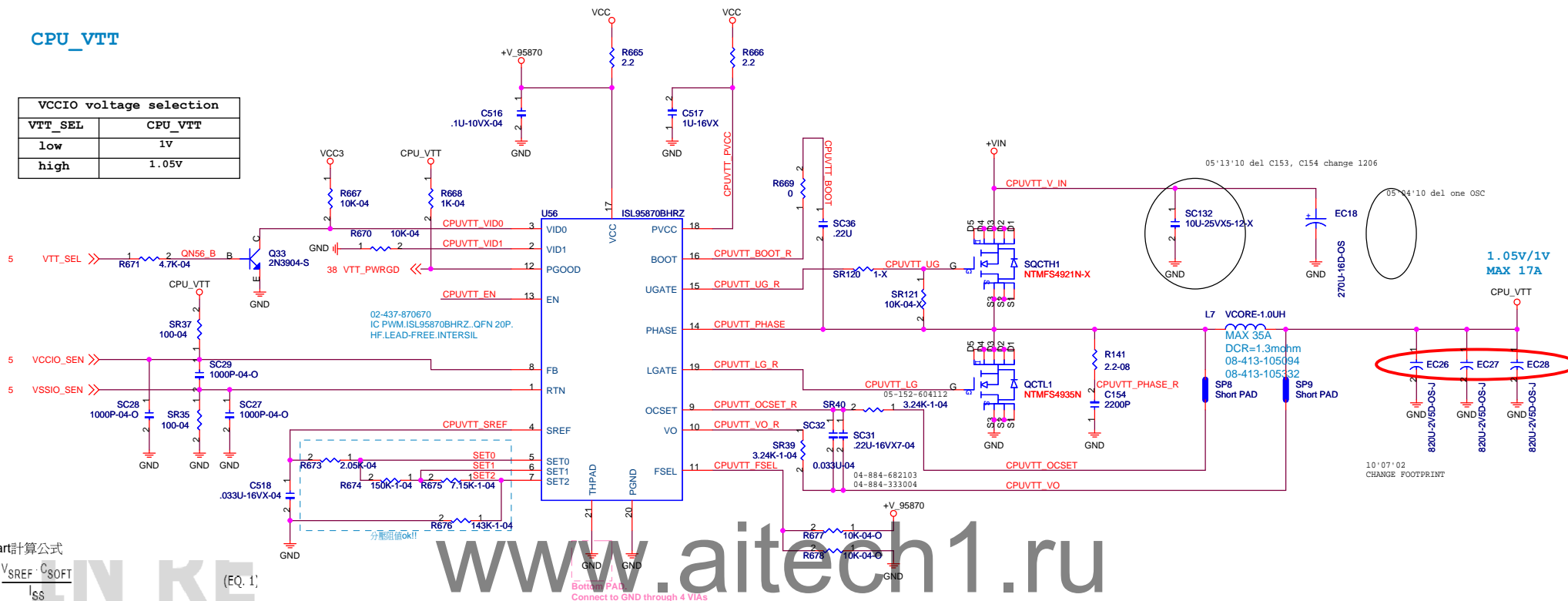


Elitegroup Computer Systems

Title	DC/DC VDIMM/DDR_VTT/5VDUAL		
Size	Document Number	Rev	
Custom	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0	
Date:	Friday, October 22, 2010	Sheet	35 of 44

CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (EQ. 1)$$

Where:

- I_{SS} is the soft-start current source at the 20μA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT			
VID1	VID0	CLOSE	V _{SREF}	V _{OUT}	
1	1	SW0	V _{SET1}	V _{OUT1}	
1	0	SW1	V _{SET2}	V _{OUT2}	
0	1	SW2	V _{SET3}	V _{OUT3}	
0	0	SW3	V _{SET4}	V _{OUT4}	

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (EQ. 21)$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad (EQ. 22)$$

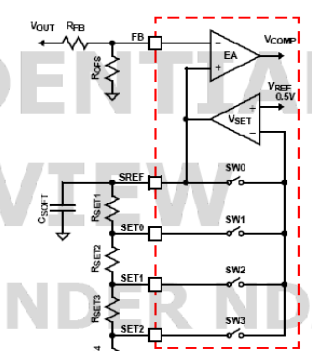
The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad (EQ. 23)$$

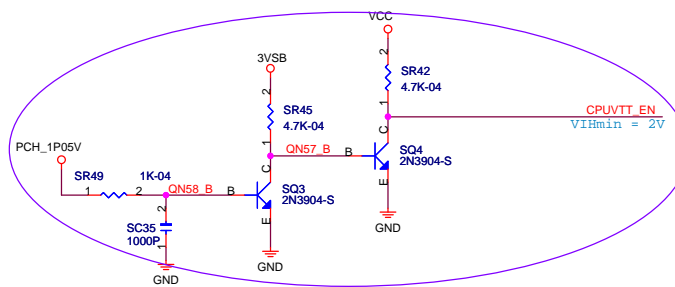
The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad (EQ. 24)$$

FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT



Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

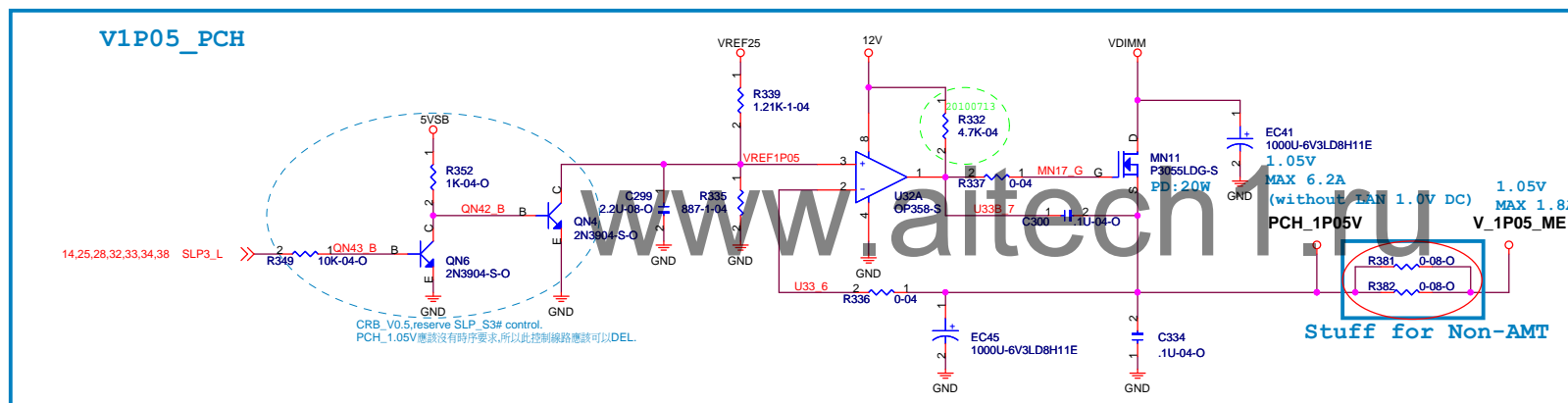
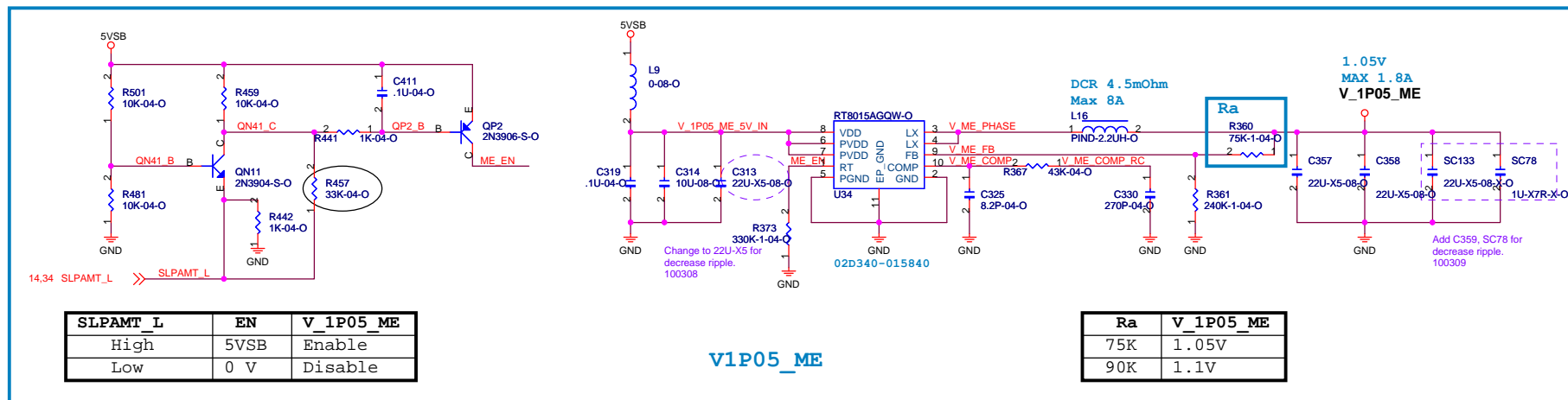


Elitegroup Computer Systems

Title: **DC/DC V_CPUVTT**

Size: Custom Document Number: **Q67H2-AD/ Q65H2-AD/ H67H2-AD** Rev: **V1.0**

Date: Friday, October 22, 2010 Sheet: 36 of 44



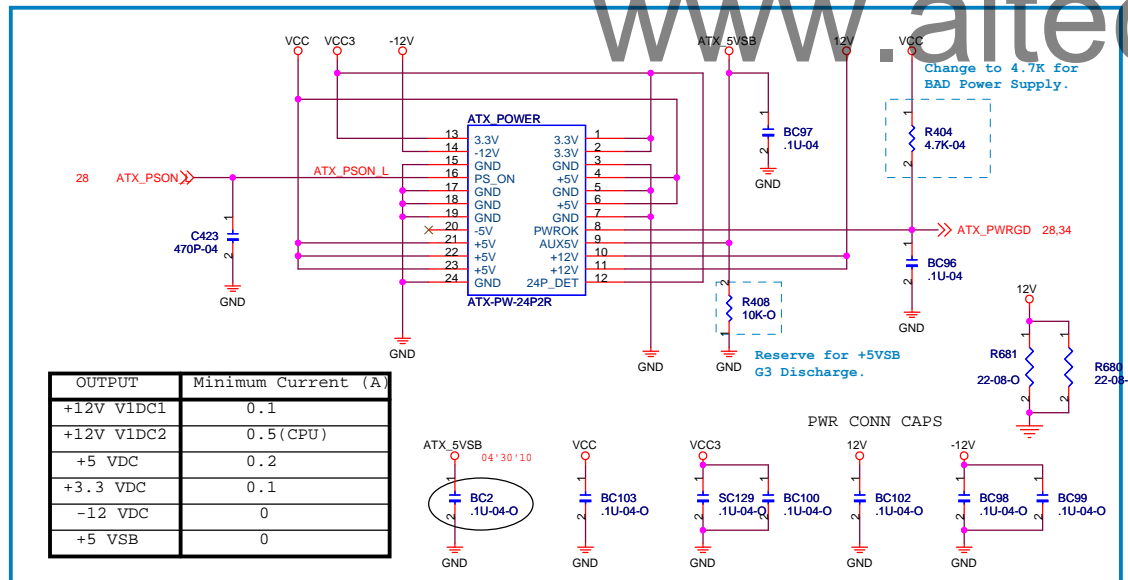
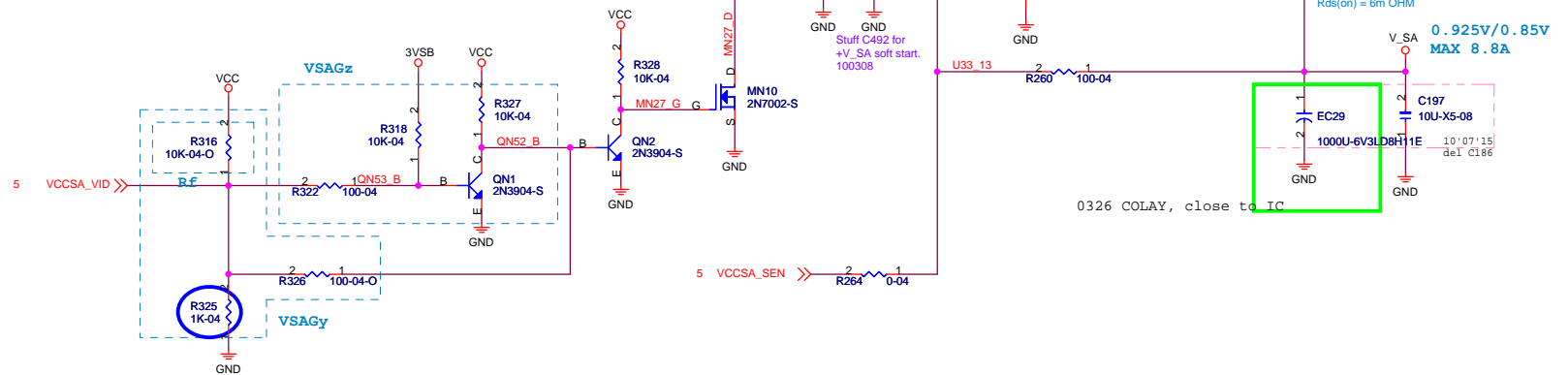
Default Stuffed:

Stuff VSAGz

VCCSA voltage selection	
VID	+V SA
0	0.925V
1	0.85V

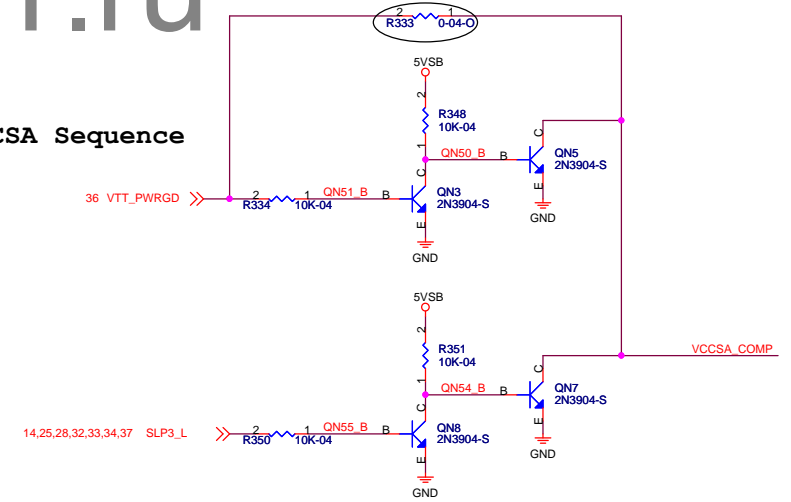
Stuff VSAGy

VCCSA voltage selection	
Rf	+V SA
unstuff	0.85V
stuff	0.925V



ATX Power 24PIN

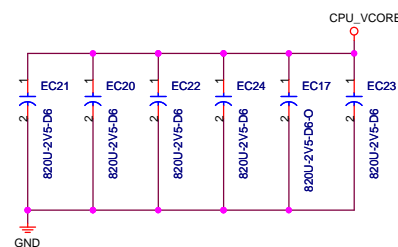
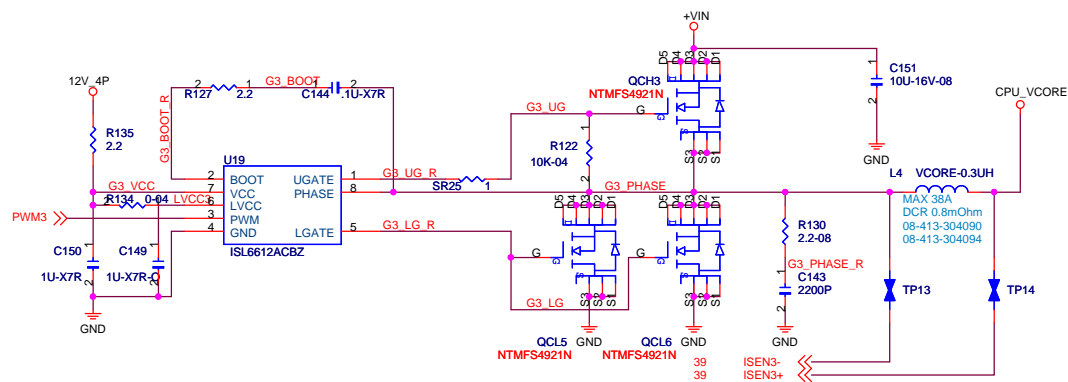
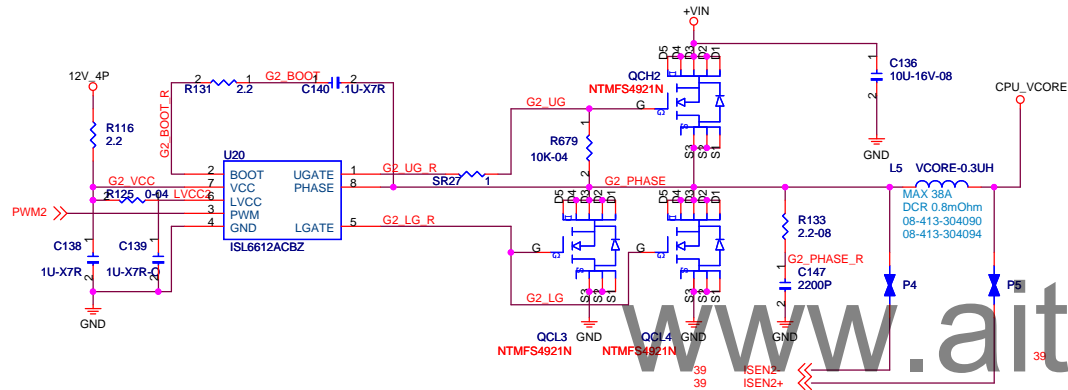
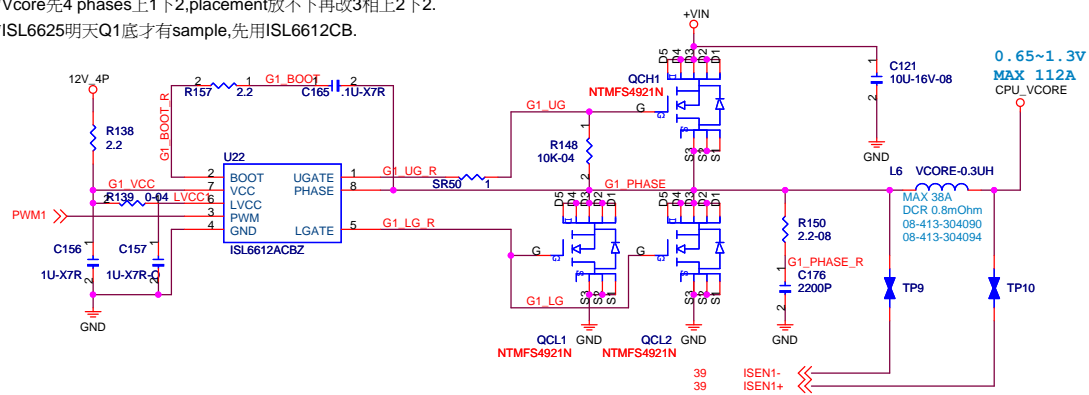
VCCSA Sequence



**Vcore先4 phases上1下2,placement放不下再改3相上2下2.

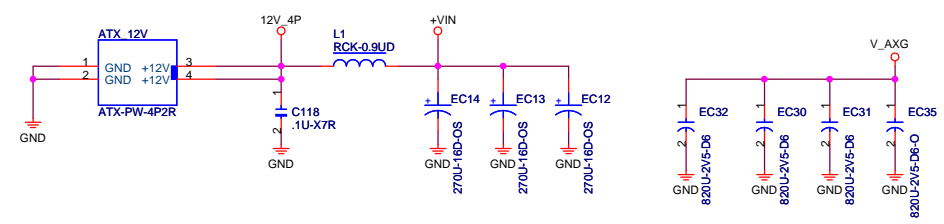
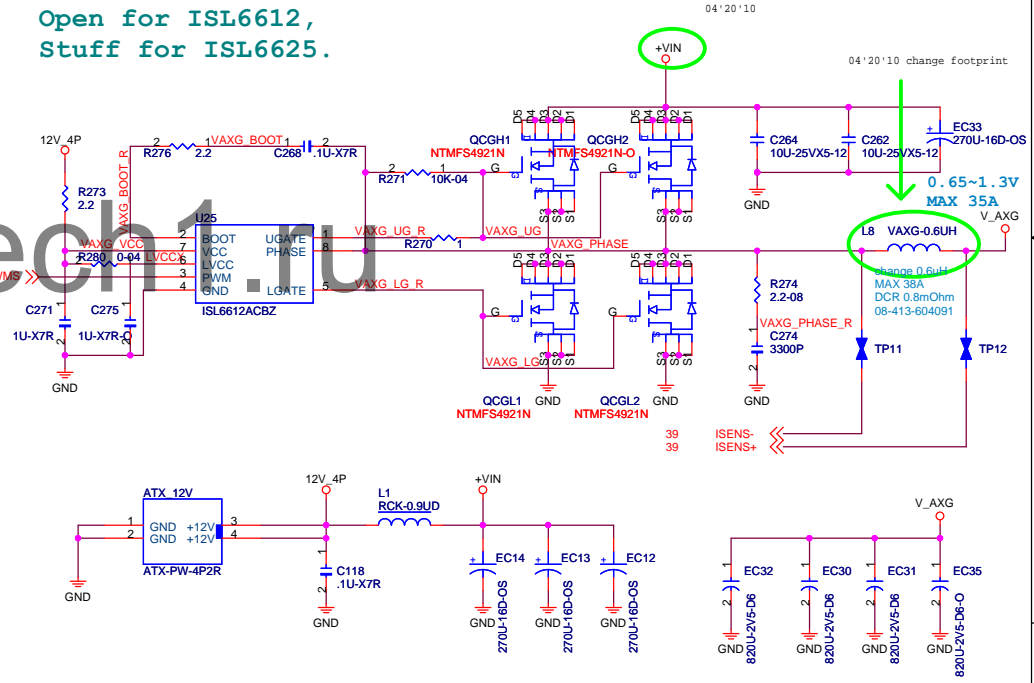
**ISL6625明天Q1底才有sample,先用ISL6612CB.

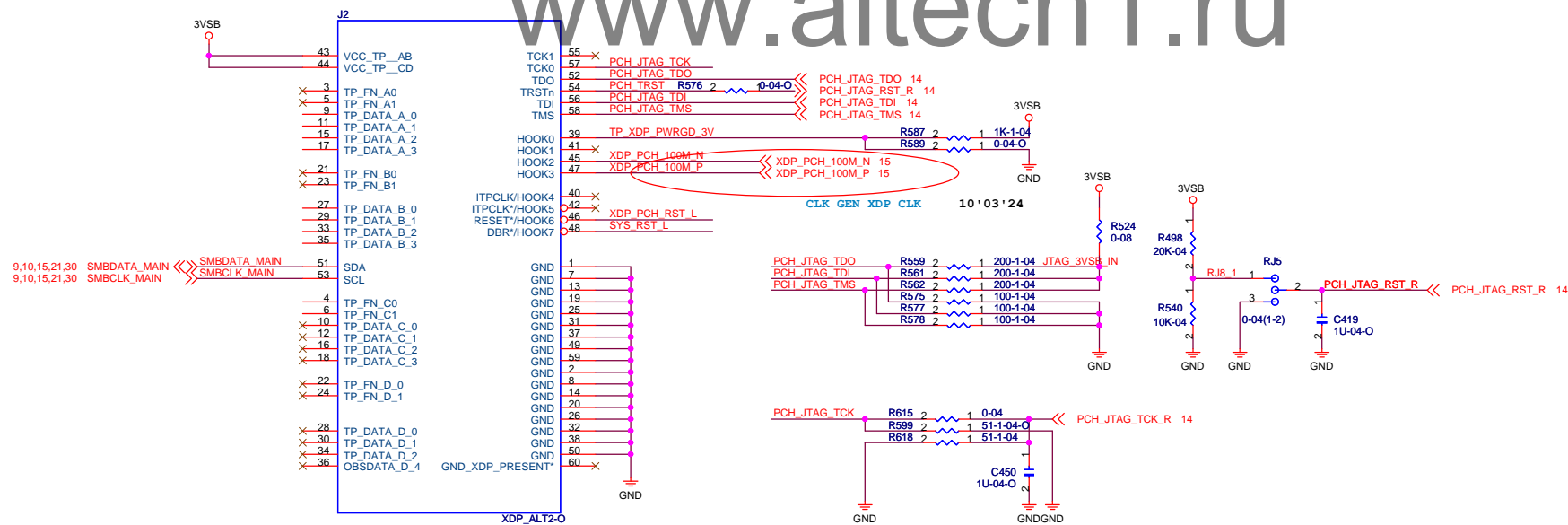
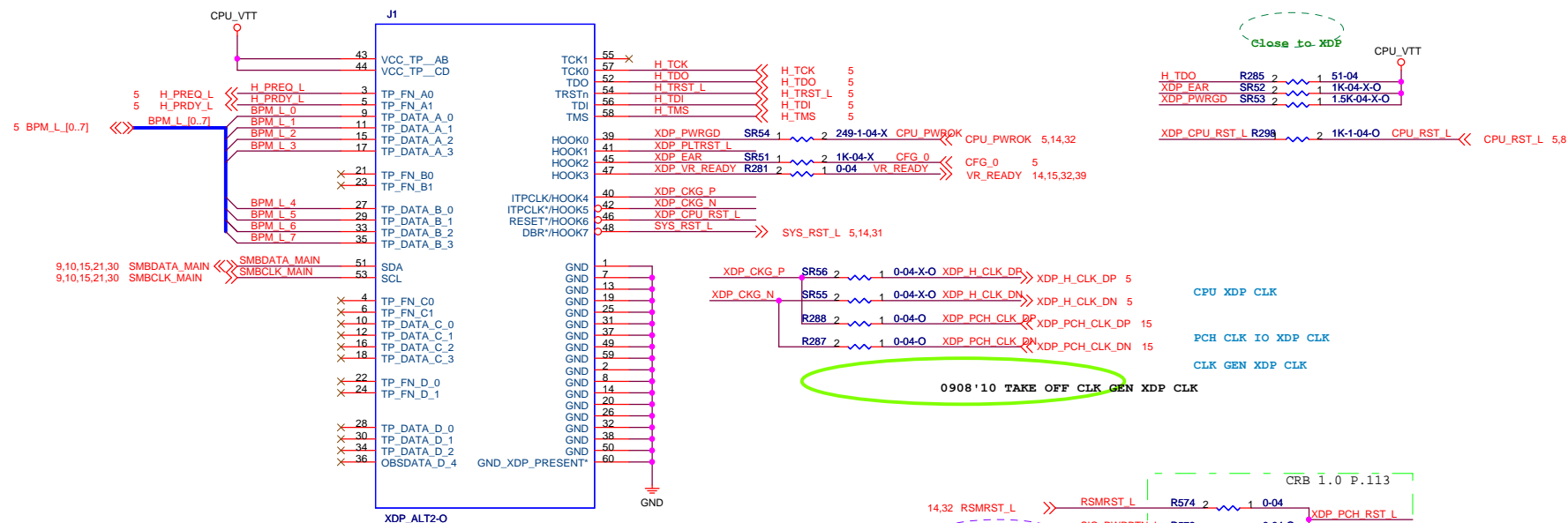
02-415-612672
IC DRIVER:ISL6612ACBZ..SO 8P,LEAD-FREE,INTERSIL



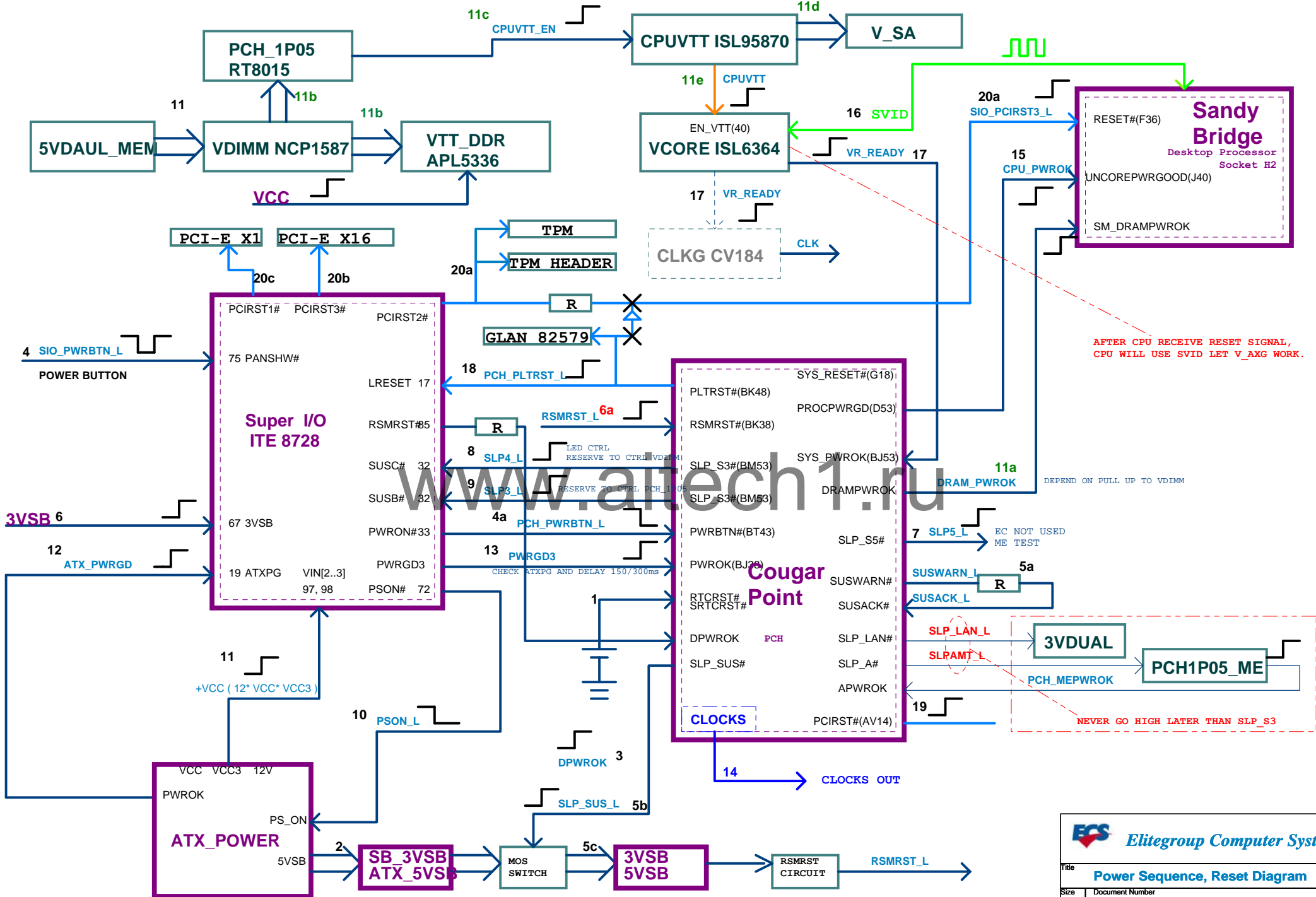
Stuff for ISL6612,
Open for ISL6625.

Open for ISL6612,
Stuff for ISL6625.





DESIGN NOTE:
PCH JTAG



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

