Q67H2-AD/ Q65H2-AD/ H67H2-AD

Rev : 1.0

TABLE OF CONTENTS

Page	Index
1	COVER PAGE
2	Block Diagram
3	GPIO Function Map
4	CPU - DMI/FDI/PEG
5	CPU - MISC
6	CPU - DDR3
7	CPU - PWR
8	GND, CPU_RST_L
9	DDR3 - CHA DIMM0/1
10	DDR3 - CHB DIMM0/1
11	DDR3 - VREF
12	PCH - DMI/PCI/PE/USB
13	PCH - SATA, SATA CONN
14	PCH - MISC, Strap Function
15	PCH - CLK IO, SLG8XP421
16	PCH - NVRAM/FDI, CLR_CMOS
17	PCH - DP/VGA
18	PCH - PWR
19	PCH - GND
20	Slot - PCI-EX16/PCI-EX1
21	SPI ROM, SMBUS
22	LAN PHY - 82579, USBLAN
23	AUDIO ALC662-VC
24	Audio Connector(PANEL)
25	USB - PWR/CONN/HDR
26	HDMI/ DVI CONNECTOR
27	VGA CONN
28	SIO IT8728F
29	FAN, COM
30	TPM, PS/2, LPT
31	F_PANEL, BUZ
32	SEQUENCE CKT
33	USB3.0 SIS 100
34	DC/DC 3VSB/3VDUAL/5VDUAL
35	DC/DC V1P05_PCH,ME/V1P8_SFR
36	DC/DC VDIMM/DDR_VTT
37	DC/DC VCCSA, ATXPWR
38	DC/DC CPU_VTT
39	DC/DC VCORE/VAXG1
40	DC/DC VCORE/VAXG2
41	XDP
42	Power Delivery
43	PWR Sequence, RST Diagram
44	Clock Distribution

NOTE:

REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/22	Initial version
V.B	2010/08/24	
V.C	2010/09/10	
V.1.0	2010/09/16	

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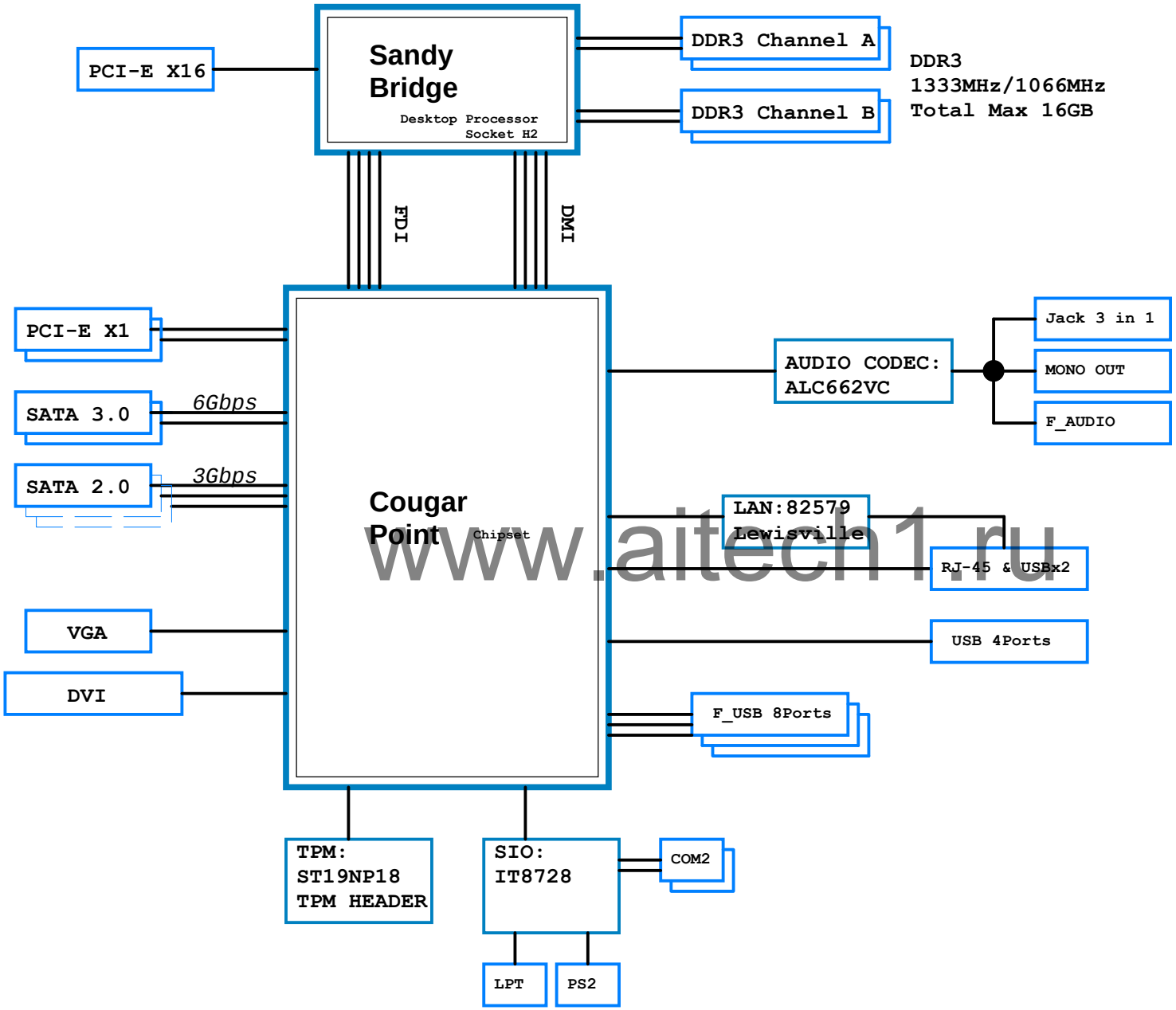
Title	Cover Page	
Size: Custom	Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD	Rev: V1.0
Date: Friday, October 22, 2010	Sheet 1 of 44	



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Title: Block Diagram

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Date: Friday, October 22, 2010 | Sheet 2 of 44

PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	LPT Detect	GPI
GPIO22	VCC3	CLR_CMOS	GPI
GPIO38	VCC3	KM Detect	GPI
GPIO39	VCC3	SENSE_Header	GPI
GPIO48	VCC3	SENSE_Header	GPI
GPIO21	VCC3	COM2 Detect	GPI
GPIO36	VCC3	TCM,TPM Detect	GPI
GPIO37	VCC3	TCM,TPM Detect	GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

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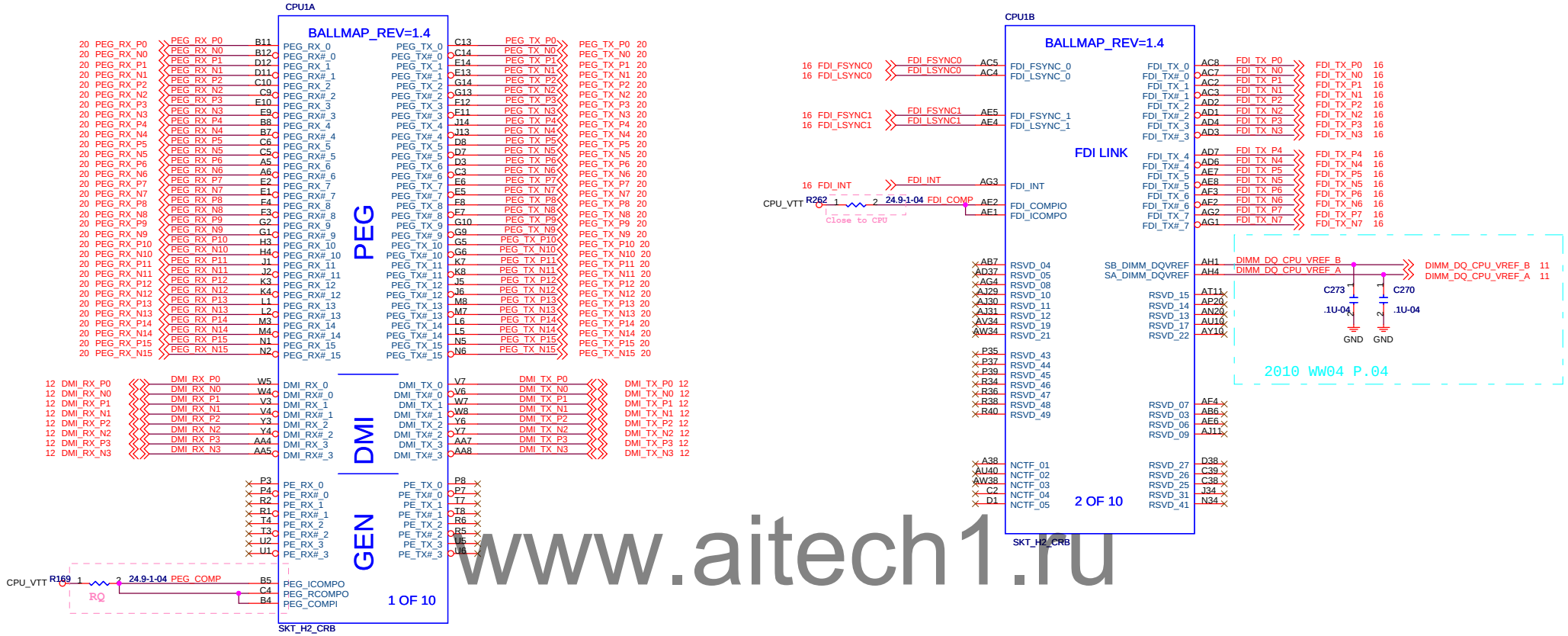

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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

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Title: CPU - DMI/FDI/PEG

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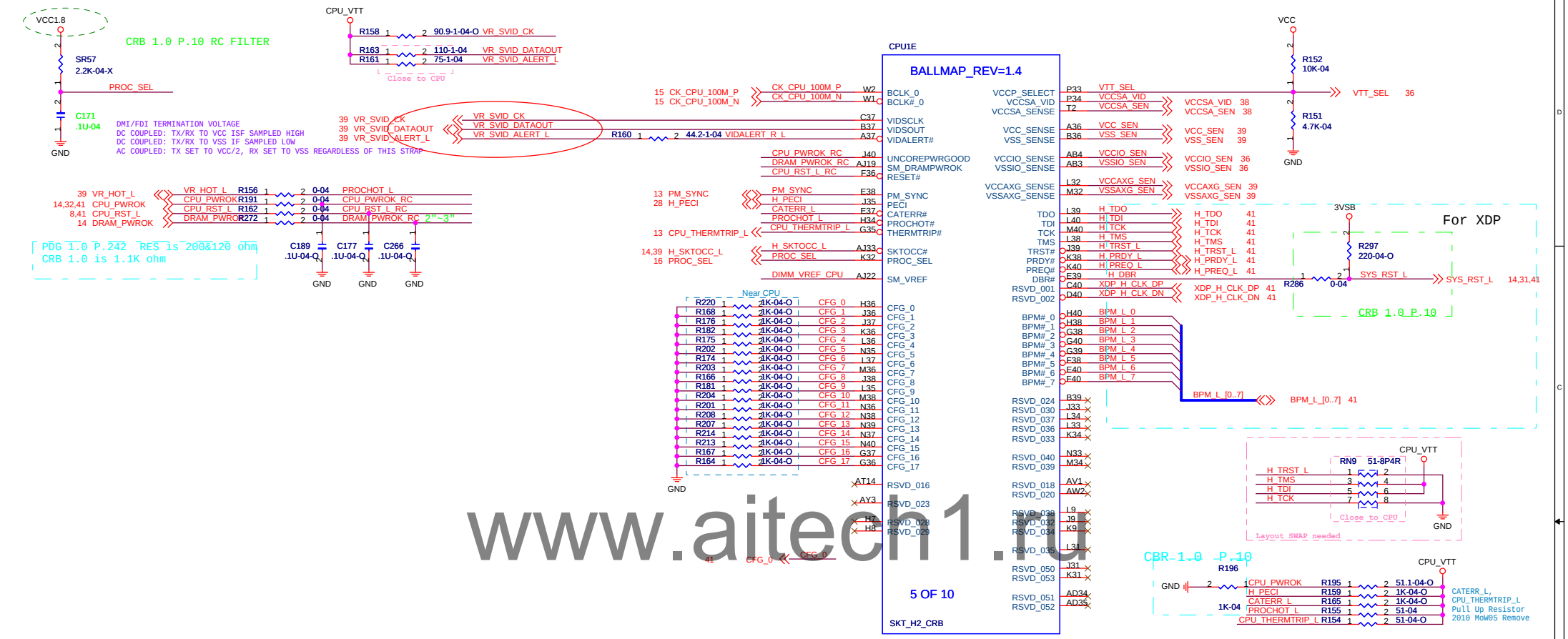
Date: Friday, October 22, 2010 | Sheet 4 of 44



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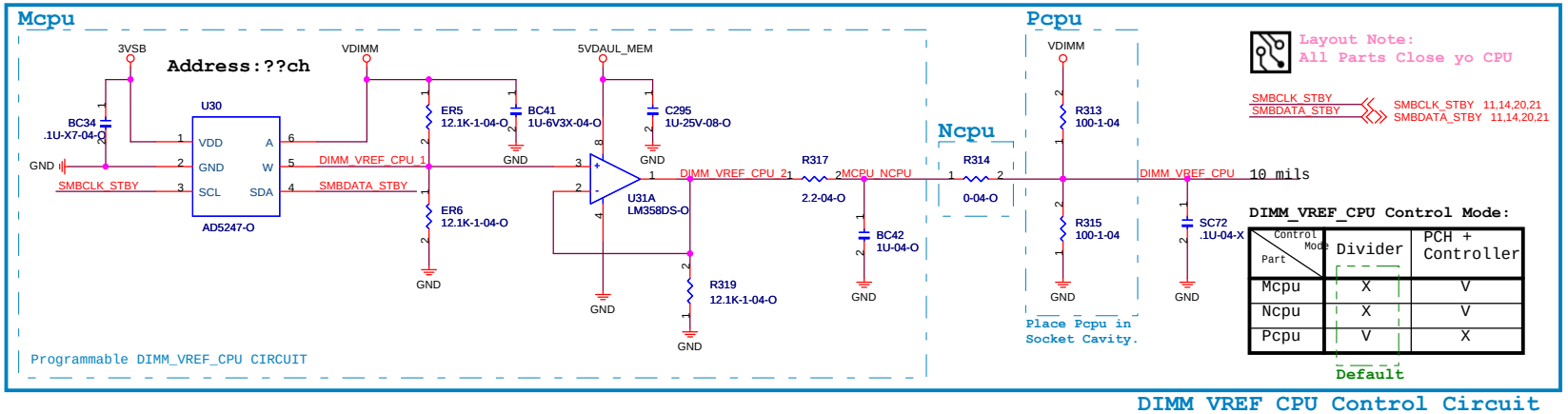
CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

*

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4



DIMM_VREF_CPU Control Circuit

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Title: CPU - MISC

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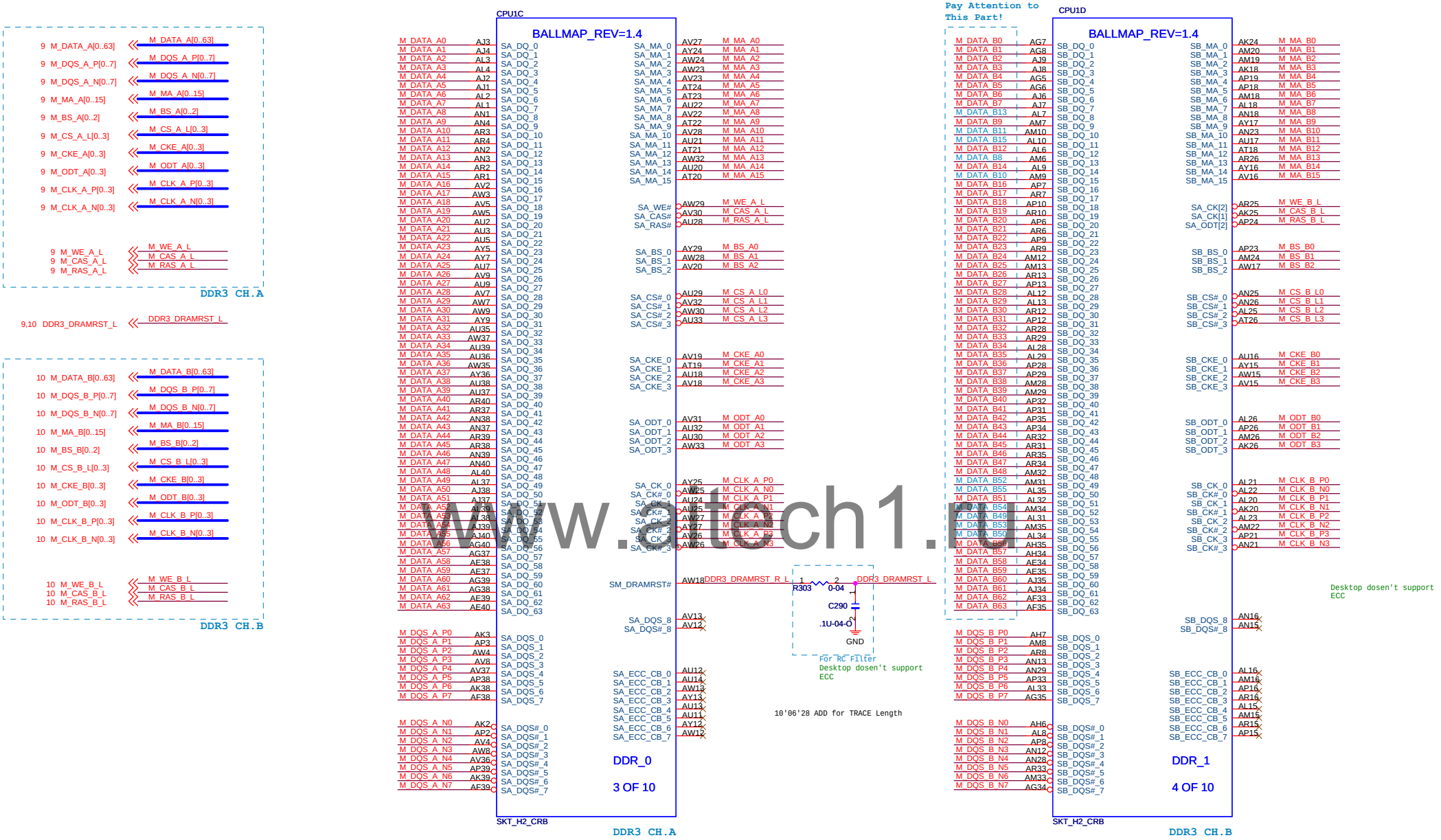
Date: Friday, October 22, 2010 | Sheet 5 of 44



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Title: CPU - DDR3

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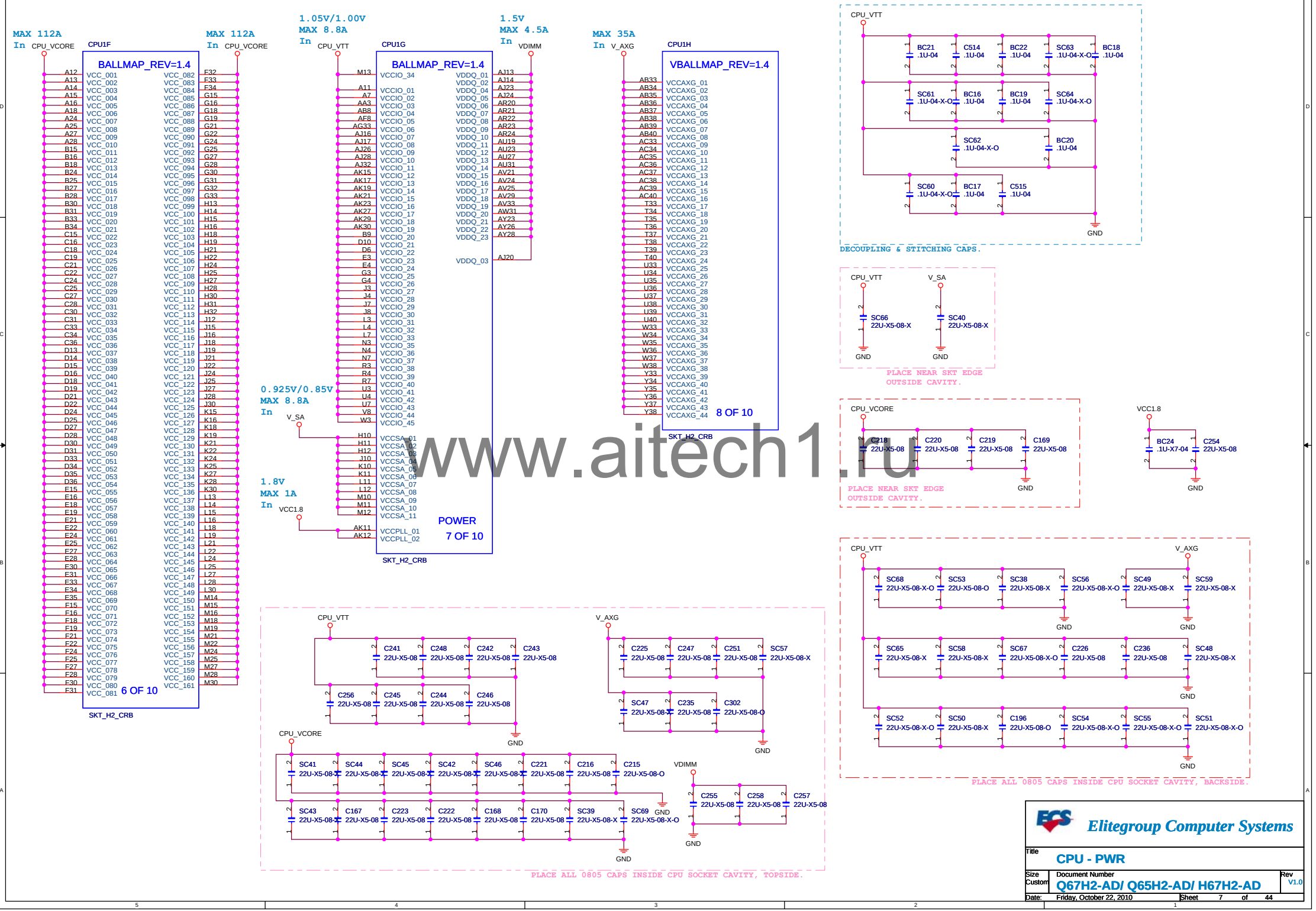
Date: Friday, October 22, 2010 | Sheet 6 of 44



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Title: CPU - PWR

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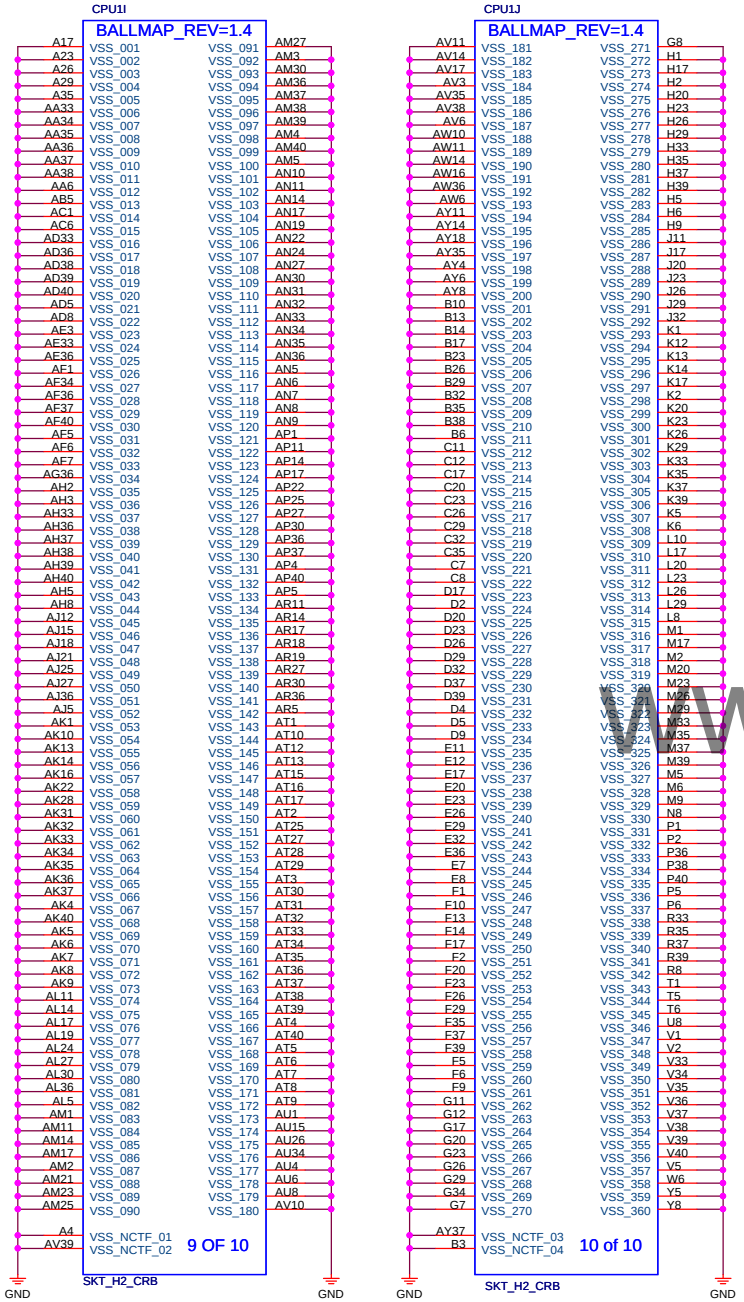
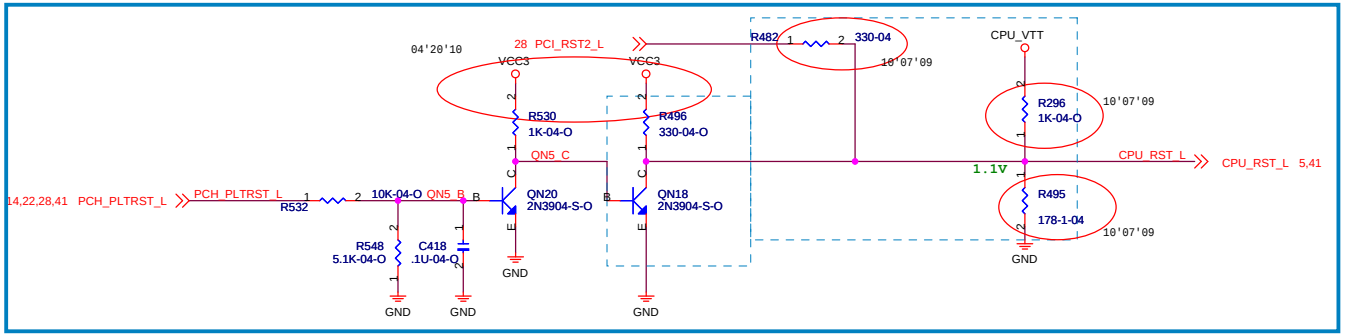
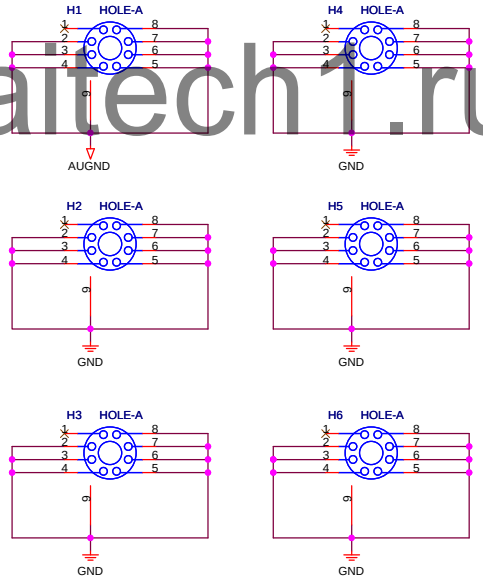
Date: Friday, October 22, 2010 | Sheet 7 of 44





PLTRST_L Driving Circuit

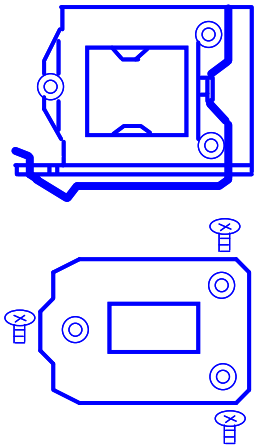
04'06'10 CHANGE FOOTPRINT



11-018-115021 CPU SMD SOCKET
SOCKET.CPU..LGA 1155p SMD.BLACK.PE115527-4041-01F.
LEAD-FREE.FOXCONN

20-800-004711 CPU SOCKET STEEL
SUBASSY.STEEL.LGA 1156P.W/
BACK PLATE.PT44A11-6401.LEAD-FREE(RoHS).FOXCONN

CPU(104)
CPU_SUBASSY_STEEL



01D201-000060 PCH ES0

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Title: CPU - GND, CPU_RST_L

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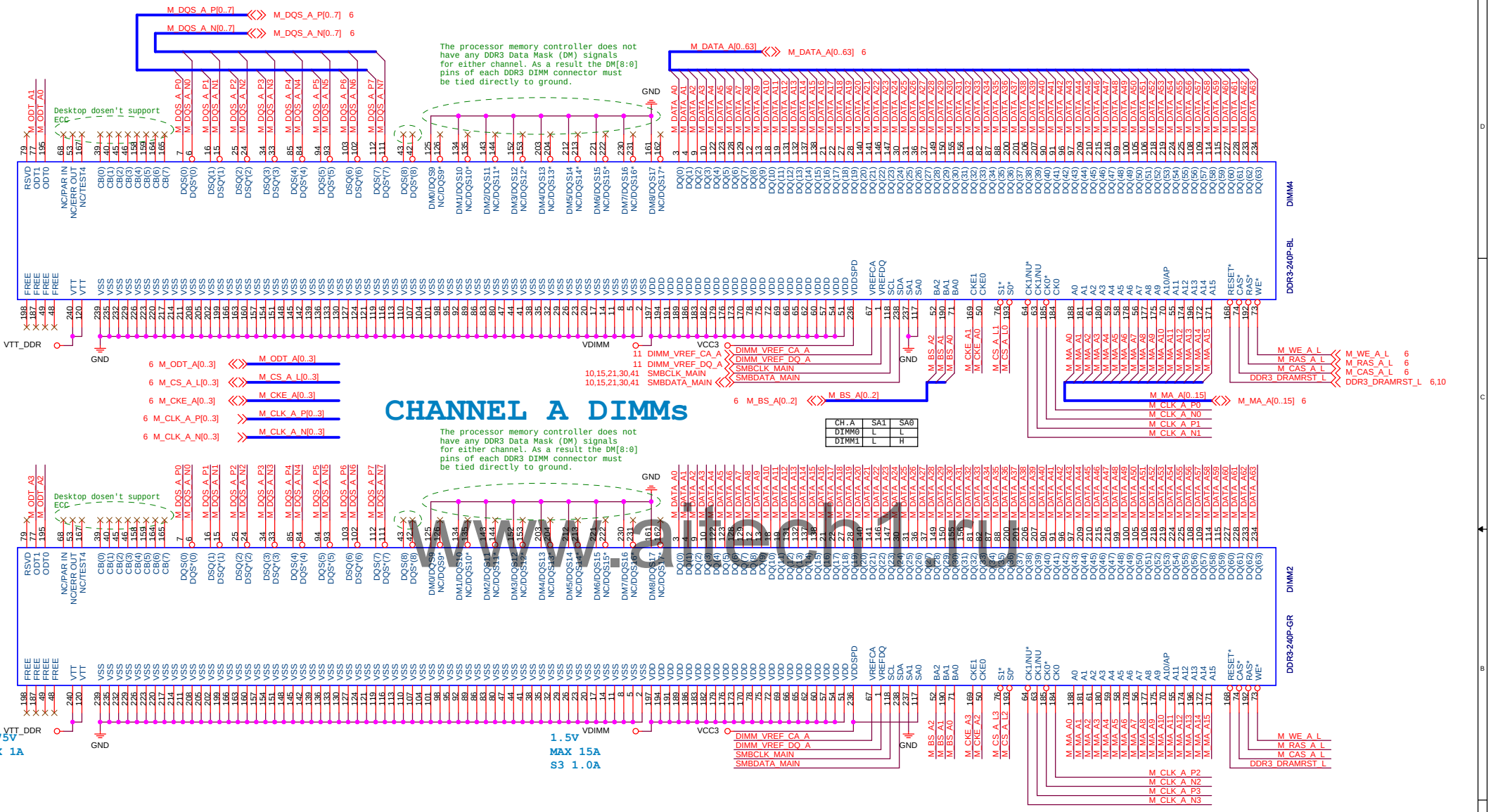
Date: Friday, October 22, 2010 | Sheet 8 of 44



CH.A	SA1	SA0
DIMM0	L	L
DIMM1	L	H

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Title: DDR3 - CHA DIMM0/1

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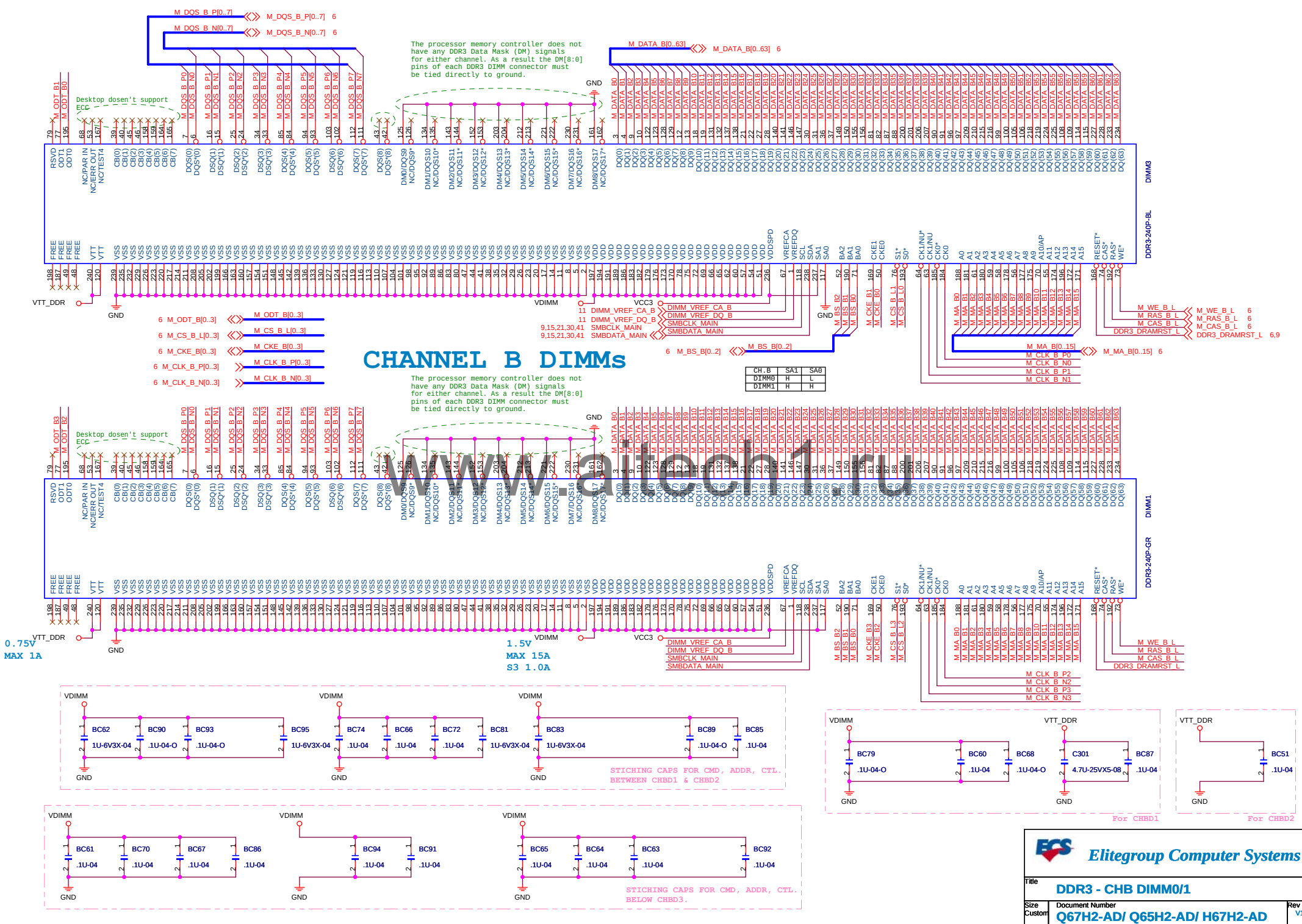
Date: Friday, October 22, 2010 | Sheet 9 of 44



CH.B	SA1	SA0
DIMM0	H	L
DIMM1	H	H

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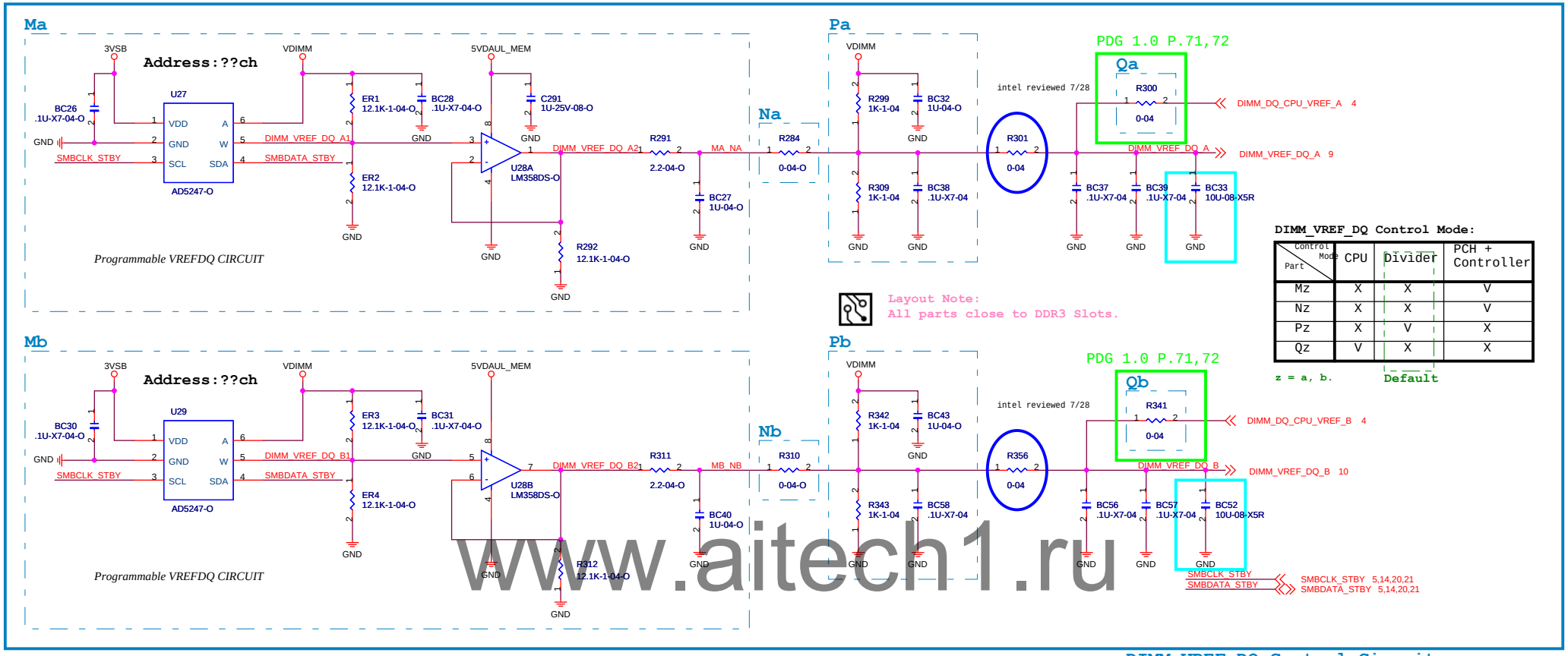
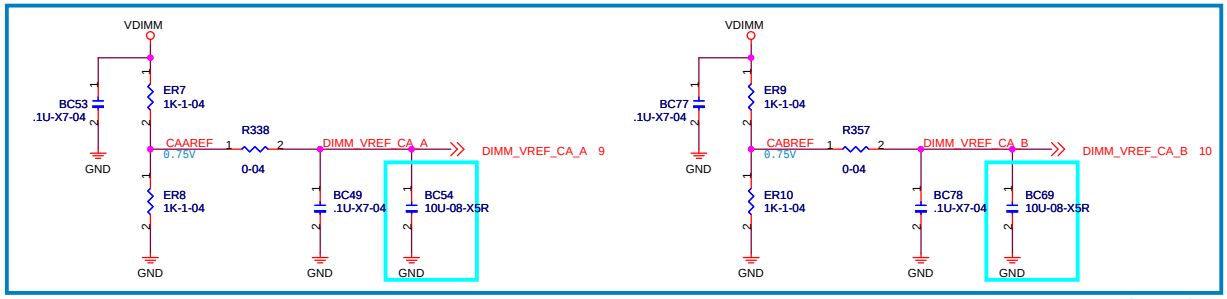


DIMM_VREF_DQ Control Mode:

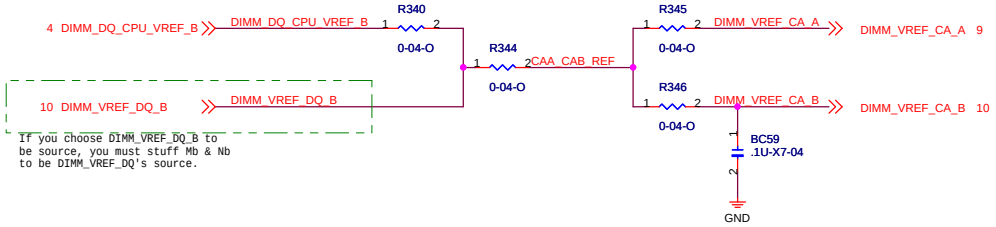
Control Mode / Part	CPU	Divider	PCH + Controller
Mz	X	X	V
Nz	X	X	V
Pz	X	V	X
Qz	V	X	X

z = a, b. Default

DIMM_VREF_DQ Control Circuit



DIMM_VREF_CA Circuit



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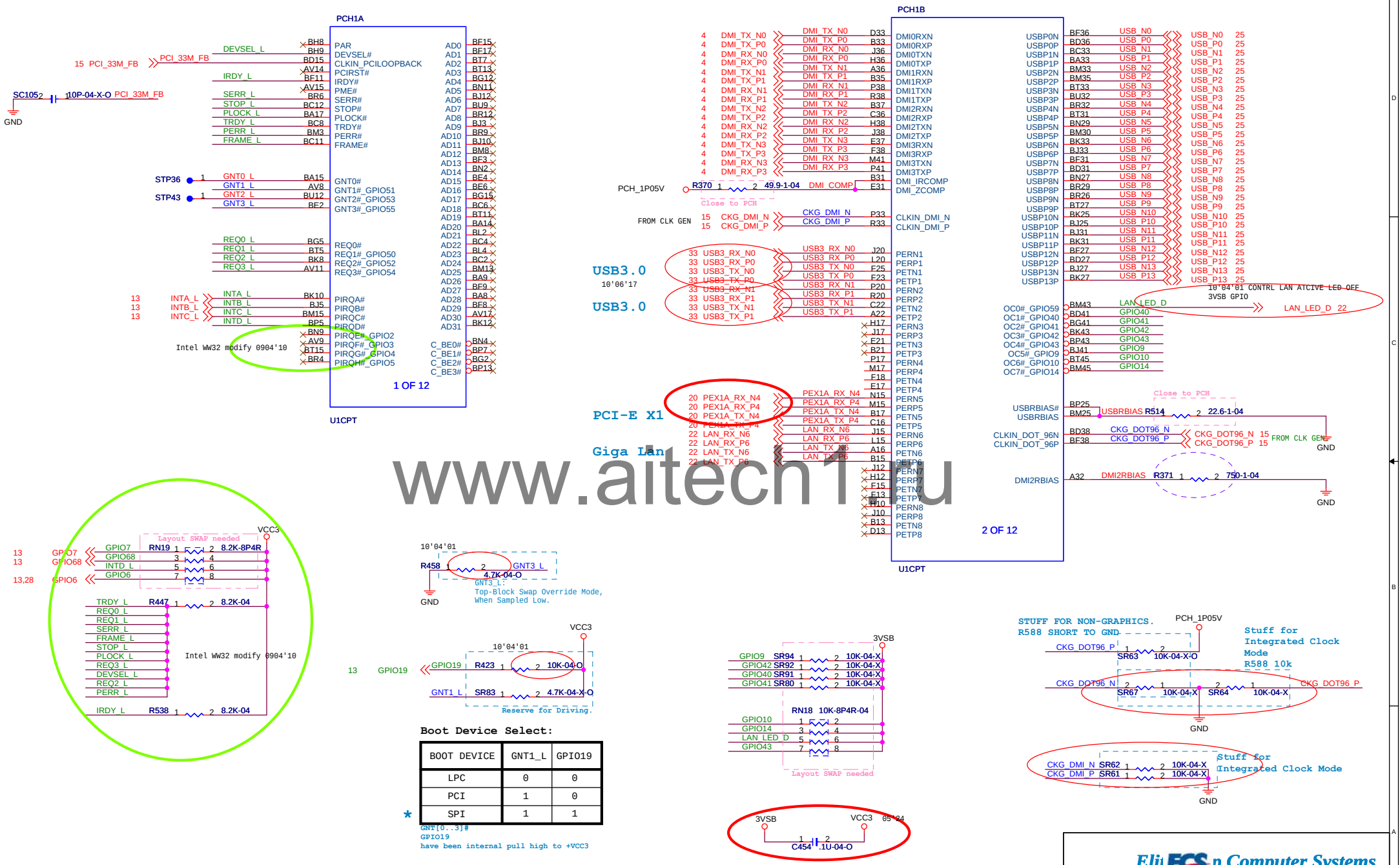
Title: DDR3 - VREF

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-A | Rev

Date: Friday, October 22, 2010 | Sheet 11 of 44



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Title: PCH - DMI/PCI/PE/USB

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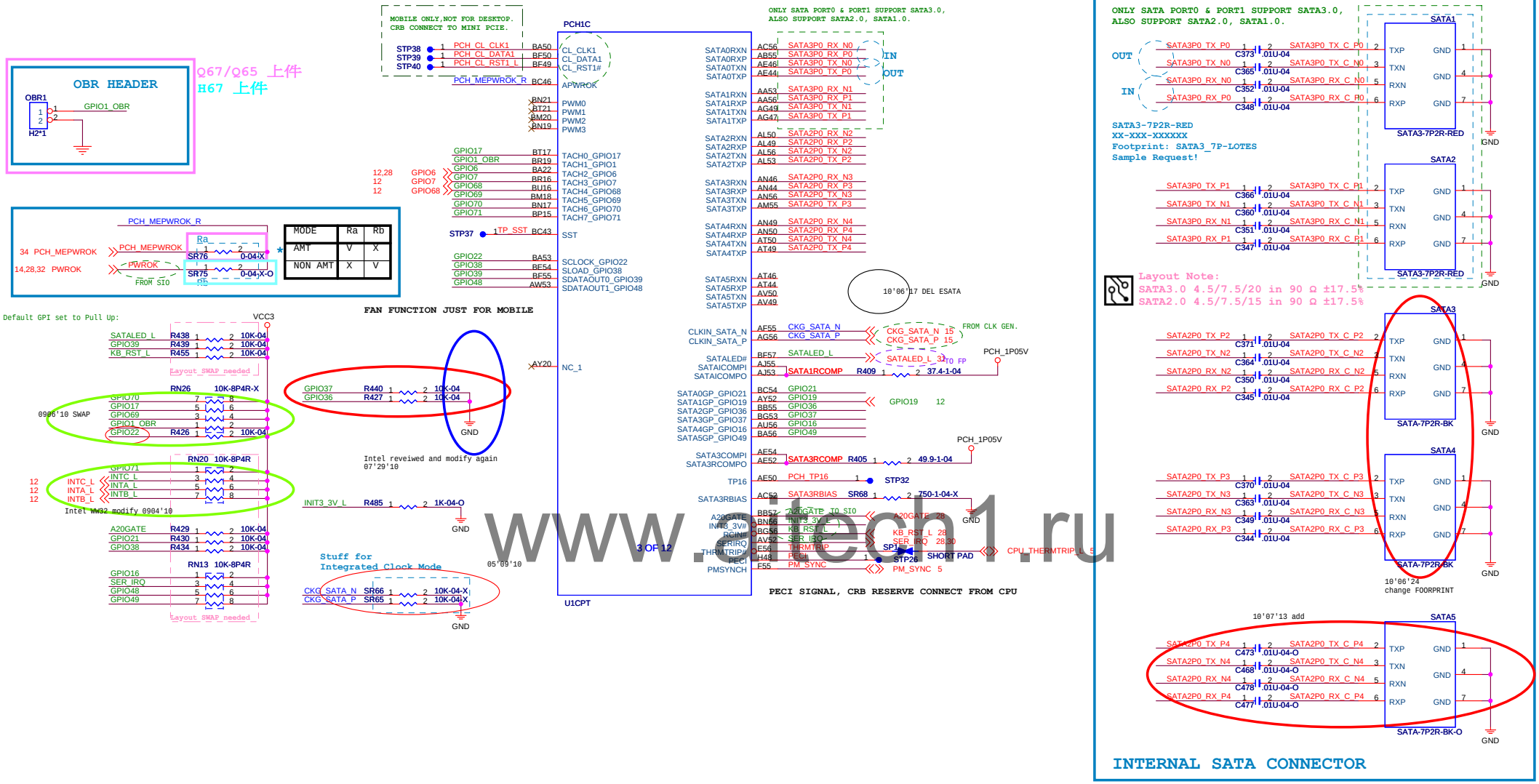
Date: Friday, October 22, 2010 | Sheet 12 of 44



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Title: PCH - SATA, SATA CONN

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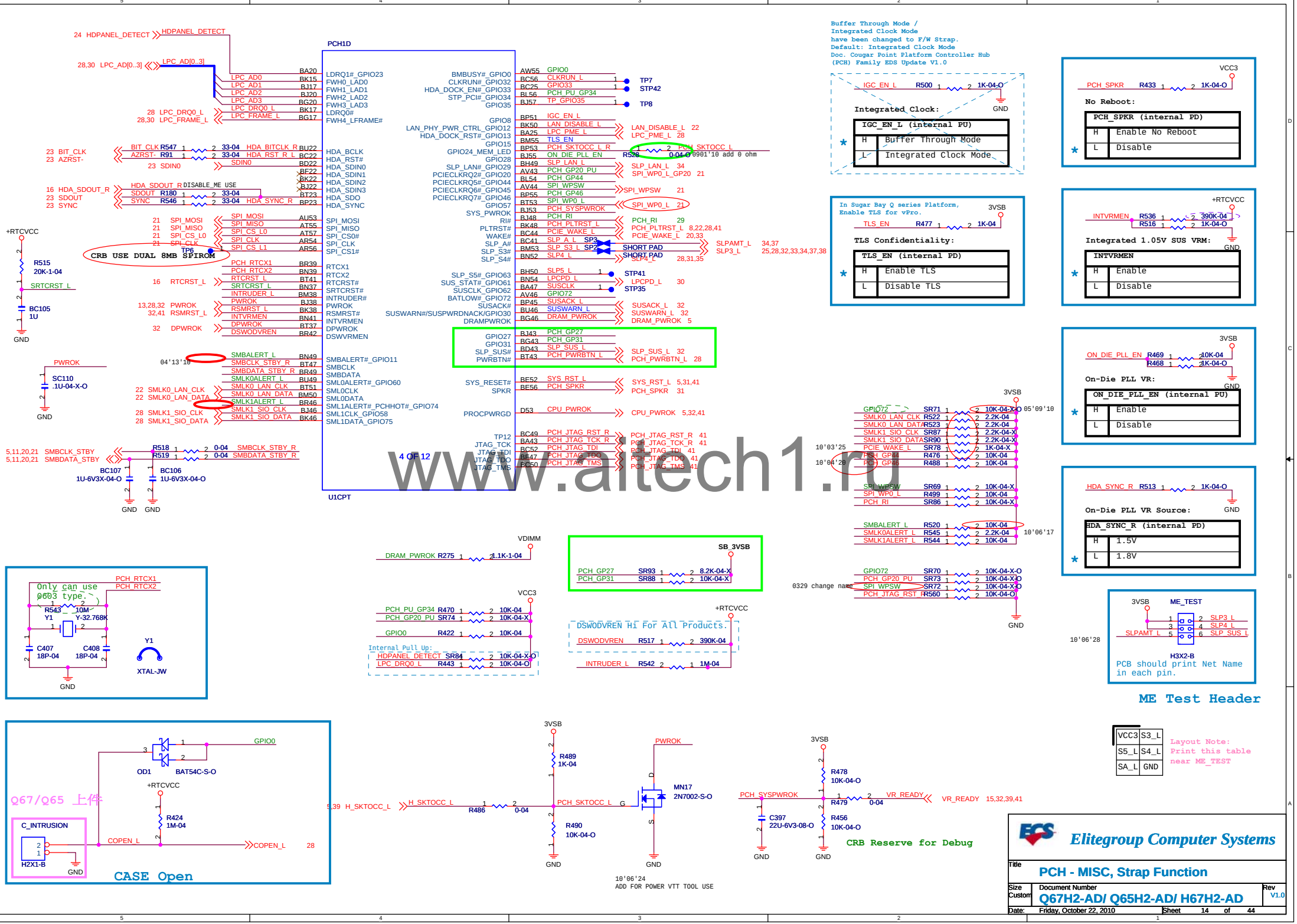
Date: Friday, October 22, 2010 | Sheet 13 of 44



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0908'10 TAKE OFF CLK GEN

CLK GEN.Seligo SLG421 Circuit.

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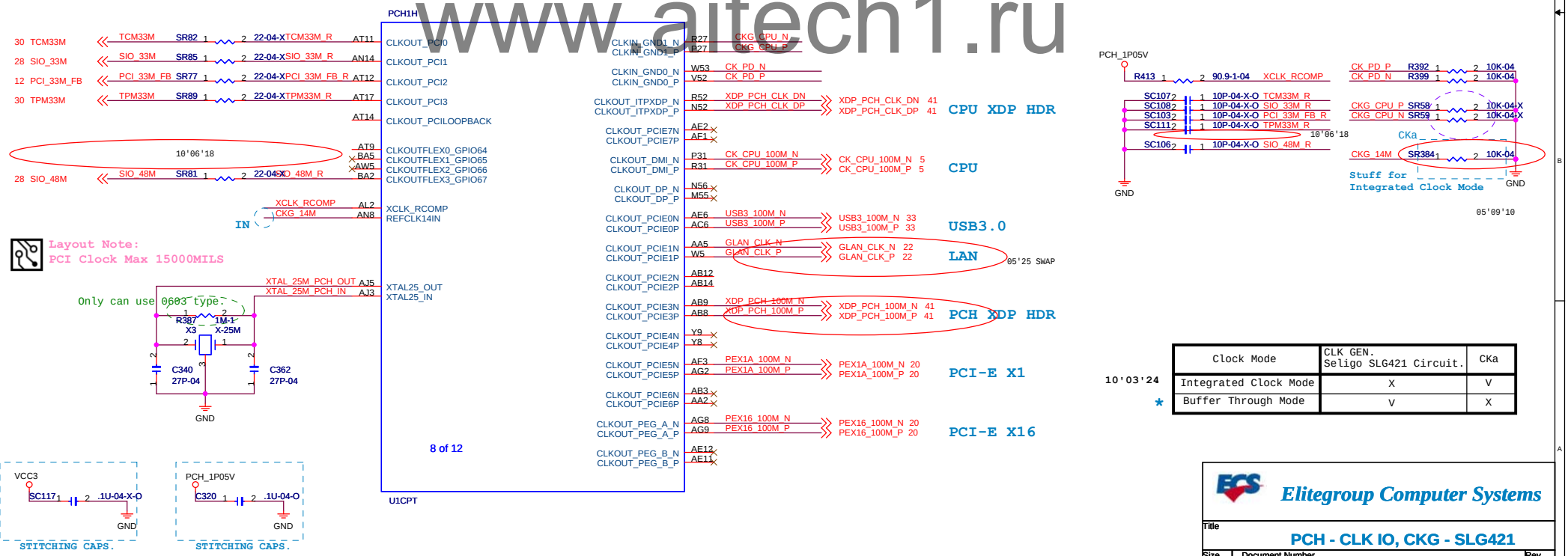

10'03'24

Clock Mode	CLK GEN. Seligo SLG421 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X

*

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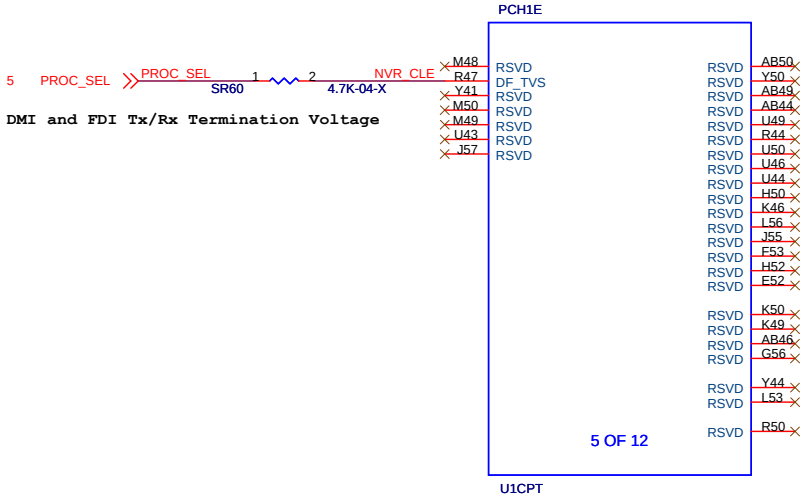
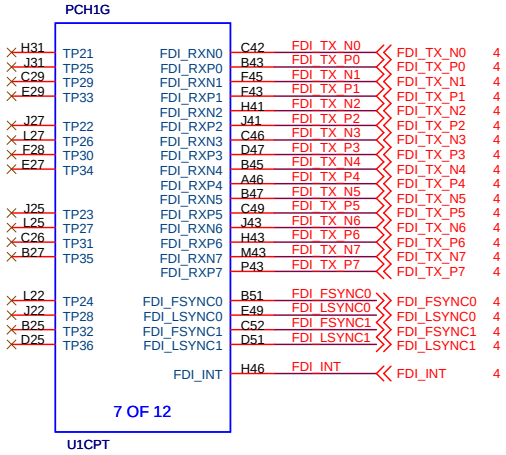
Title: PCH - CLK IO, CKG - SLG421

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 15 of 44





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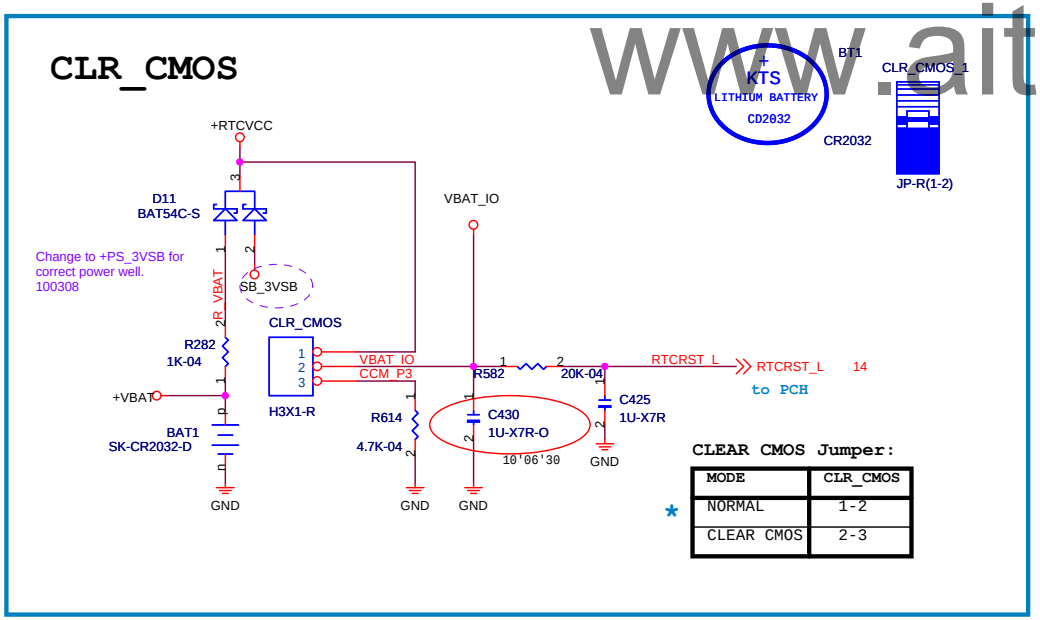
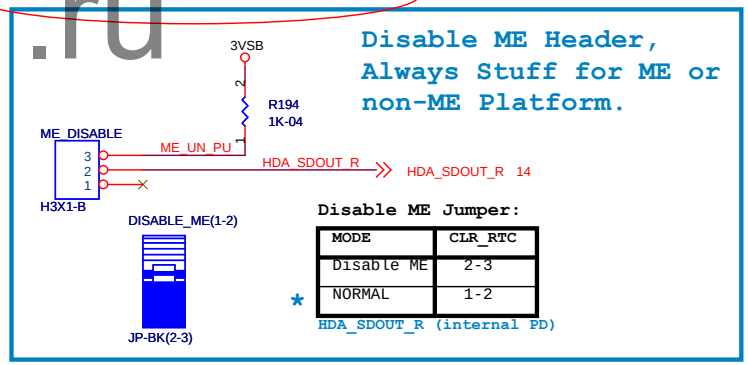


CLEAR CMOS Jumper:

MODE	CLR_CMOS
NORMAL	1-2
CLEAR CMOS	2-3

*

04'20'10 CHANGE JUMPER DEFINE



Disable ME Jumper:

MODE	CLR_RTC
Disable ME	2-3
NORMAL	1-2

*

HDA_SDOUT_R (internal PD)

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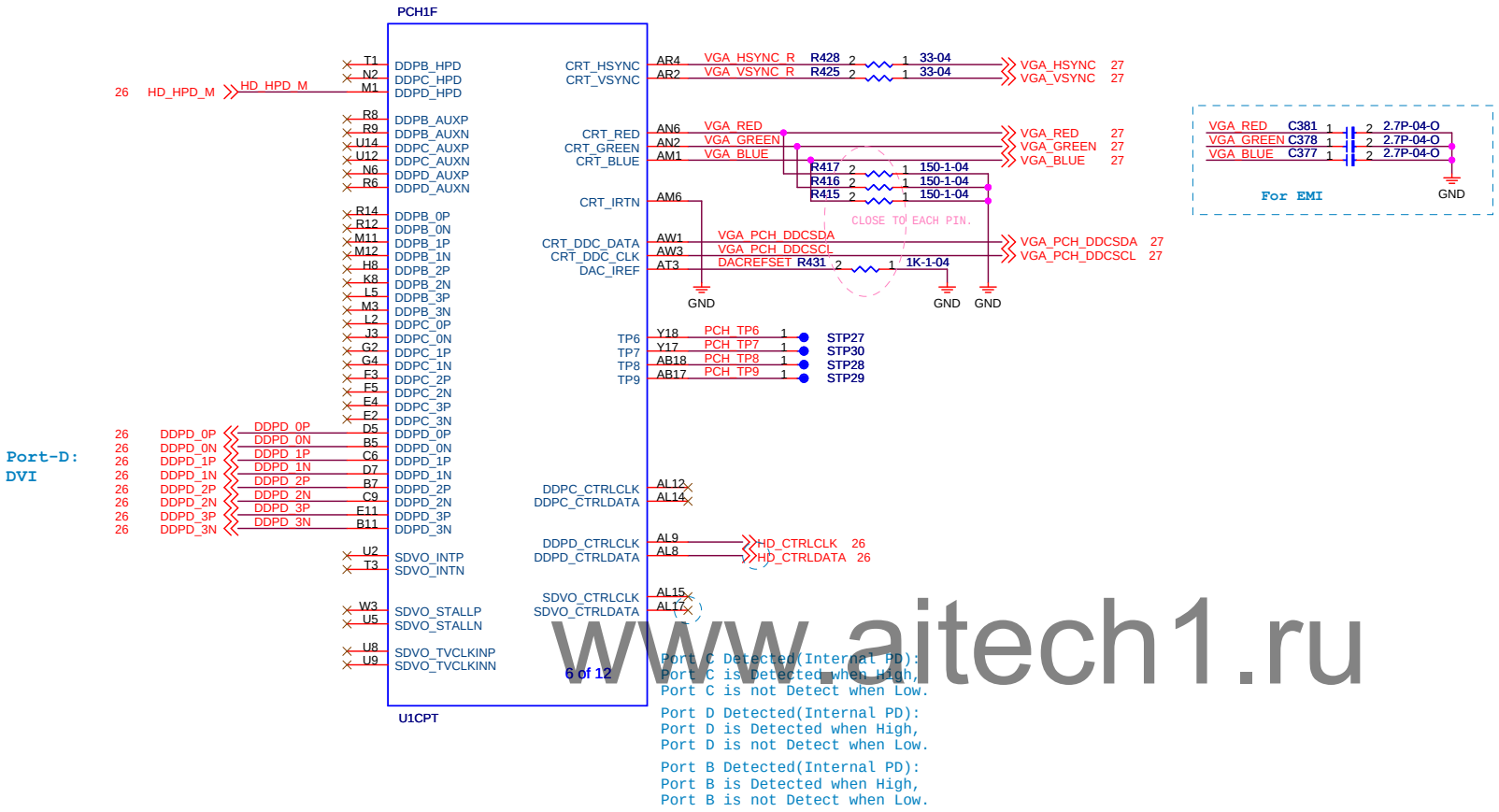
Title: PCH - NVRAM/FDI, CLR_CMOS

Size: B | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 16 of 44



Port C Detected(Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.

Port D Detected(Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.

Port B Detected(Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.

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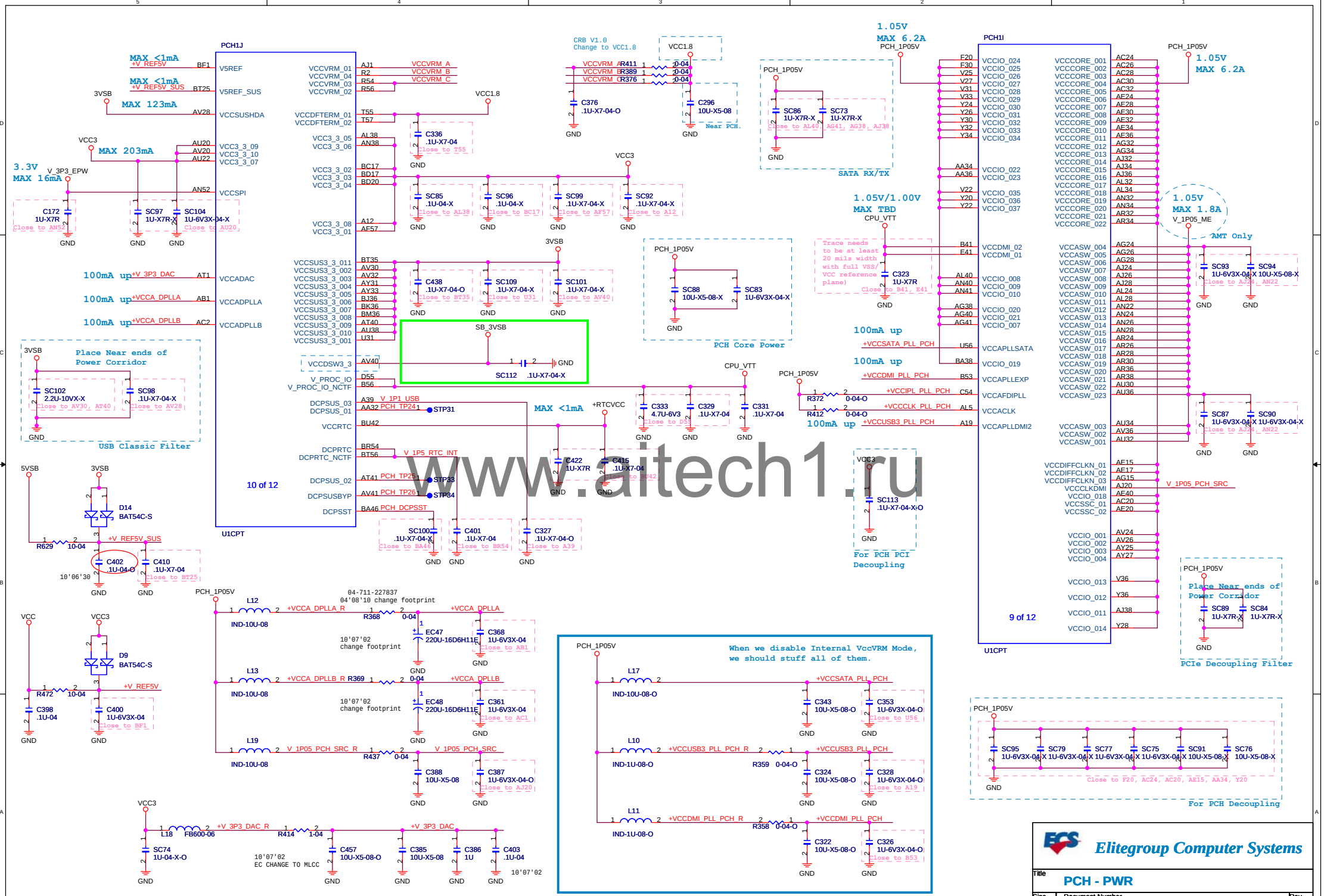
Title	PCH - DP/VGA
Size B	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD
Rev	V1.0
Date:	Friday, October 22, 2010
Sheet	17 of 44



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Title: PCH - PWR

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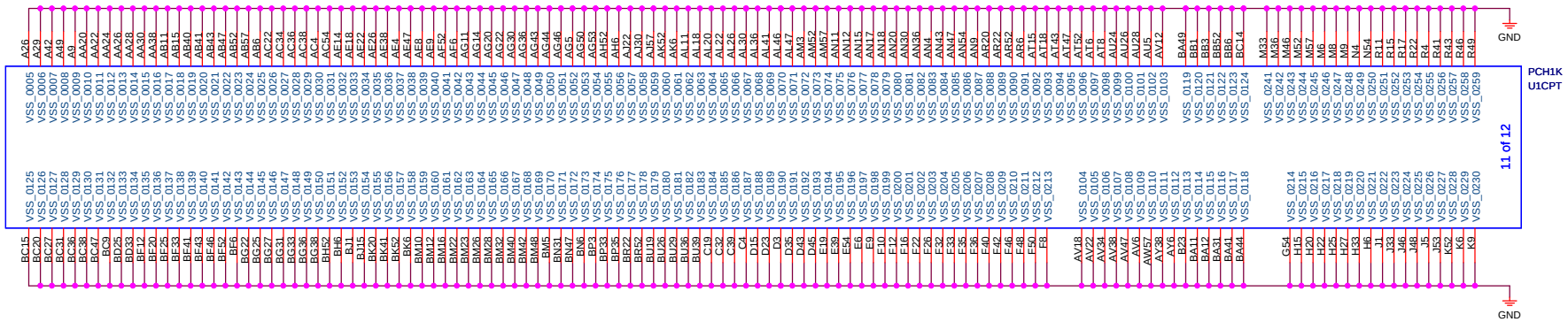
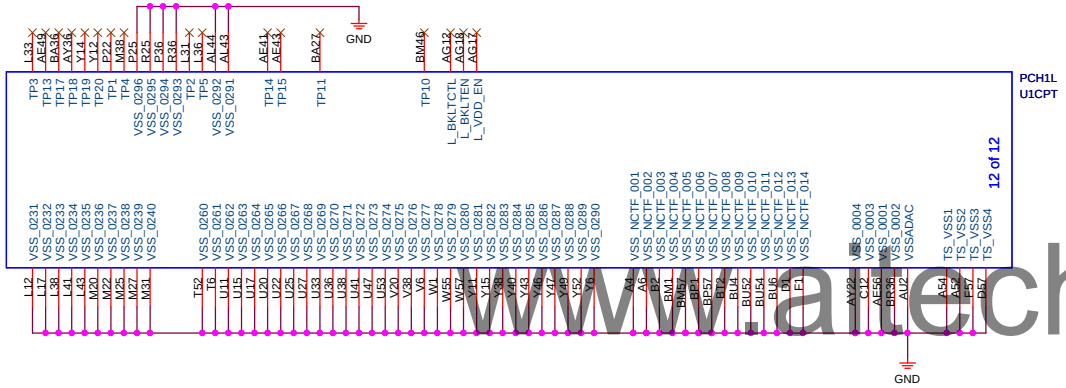
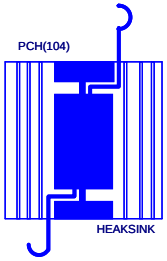
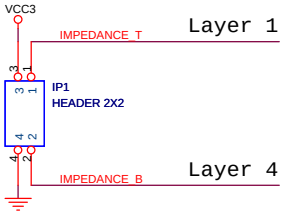
Date: Friday, October 22, 2010 | Sheet 18 of 44







2010'08'19 update heatsink footprint to hk29d4x30d7_pt40d11x21



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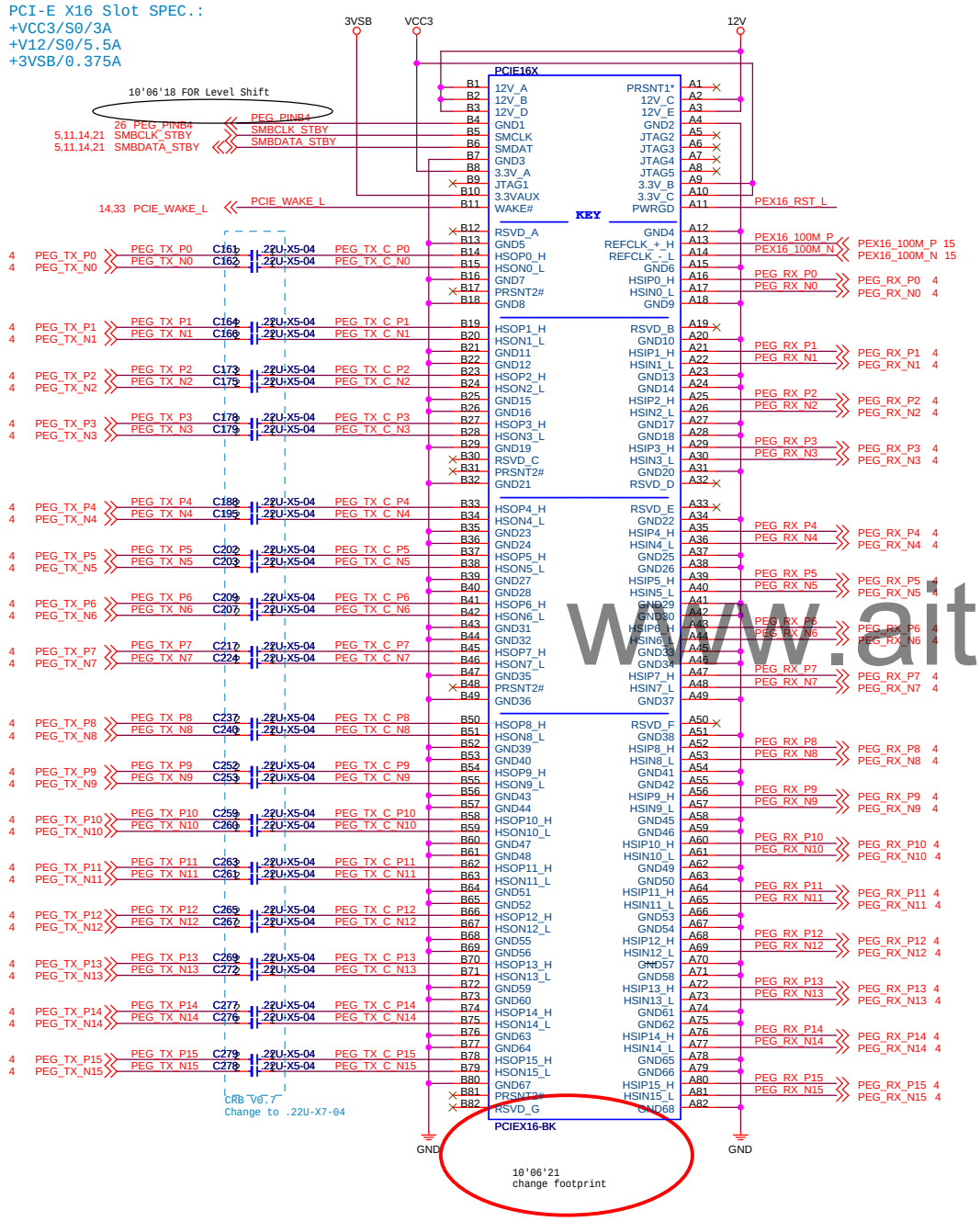
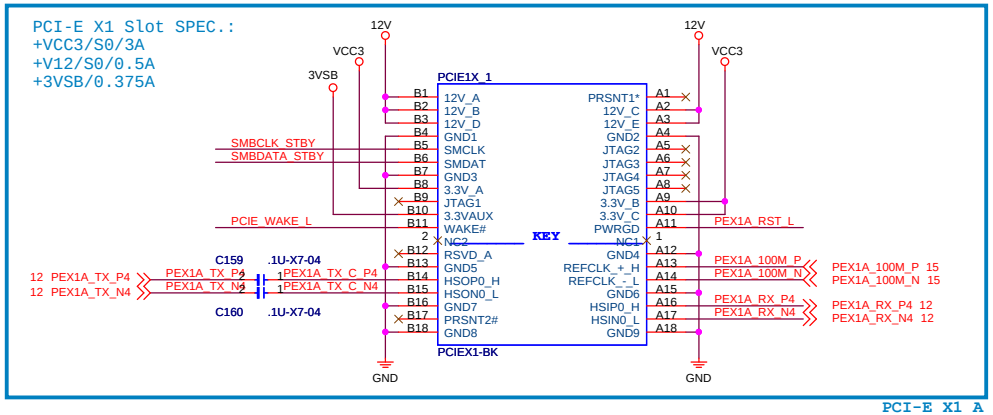
Title: PCH - GND

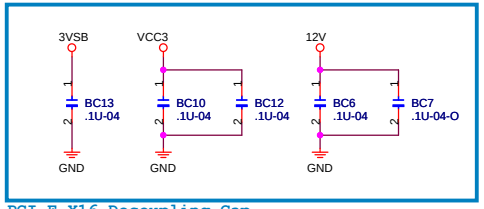
Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 19 of 44

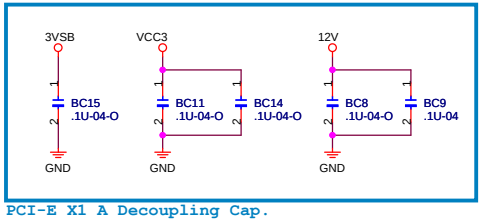




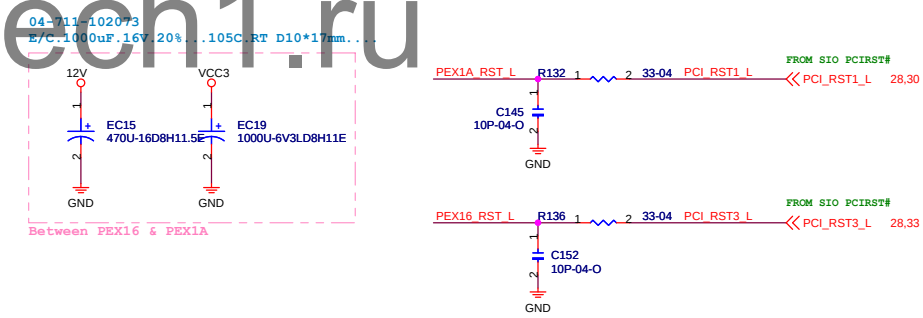
PCI-E X1 A



PCI-E X16 Decoupling Cap.



PCI-E X1 A Decoupling Cap.



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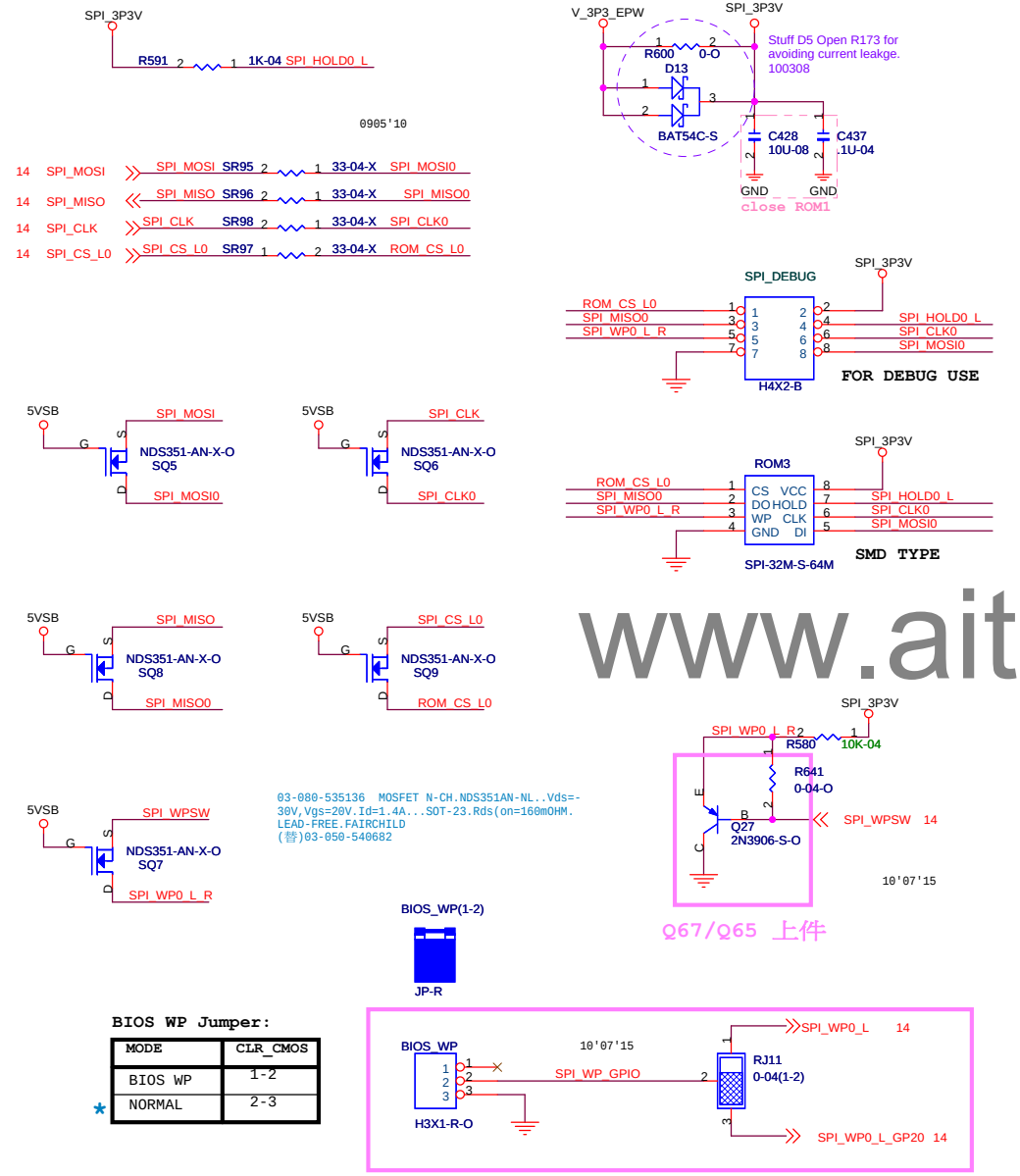
Title: Slot - PCI-EX16/PCI-EX1

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 20 of 44

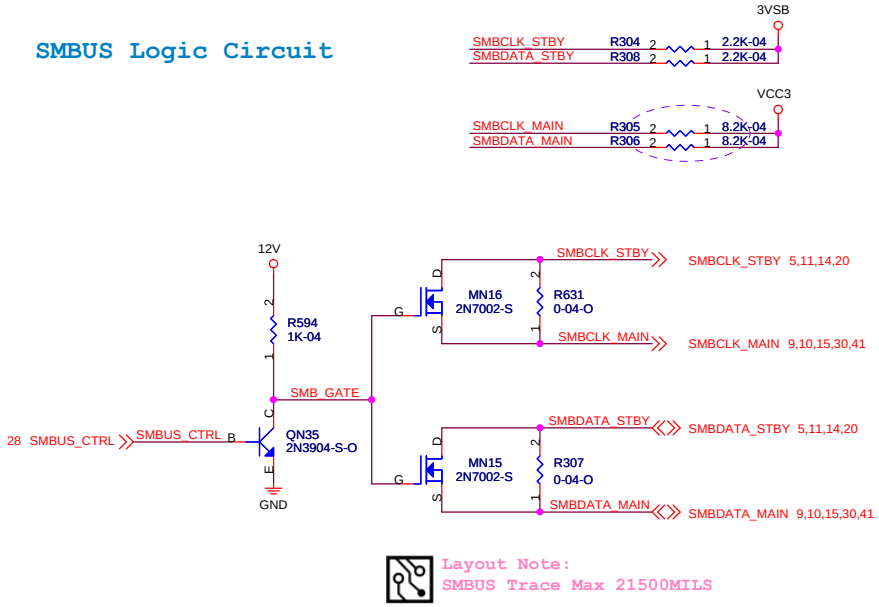
SPI ROM Circuit



BIOS WP Jumper:

MODE	CLR_CMOS
BIOS WP	1-2
* NORMAL	2-3

SMBUS Logic Circuit



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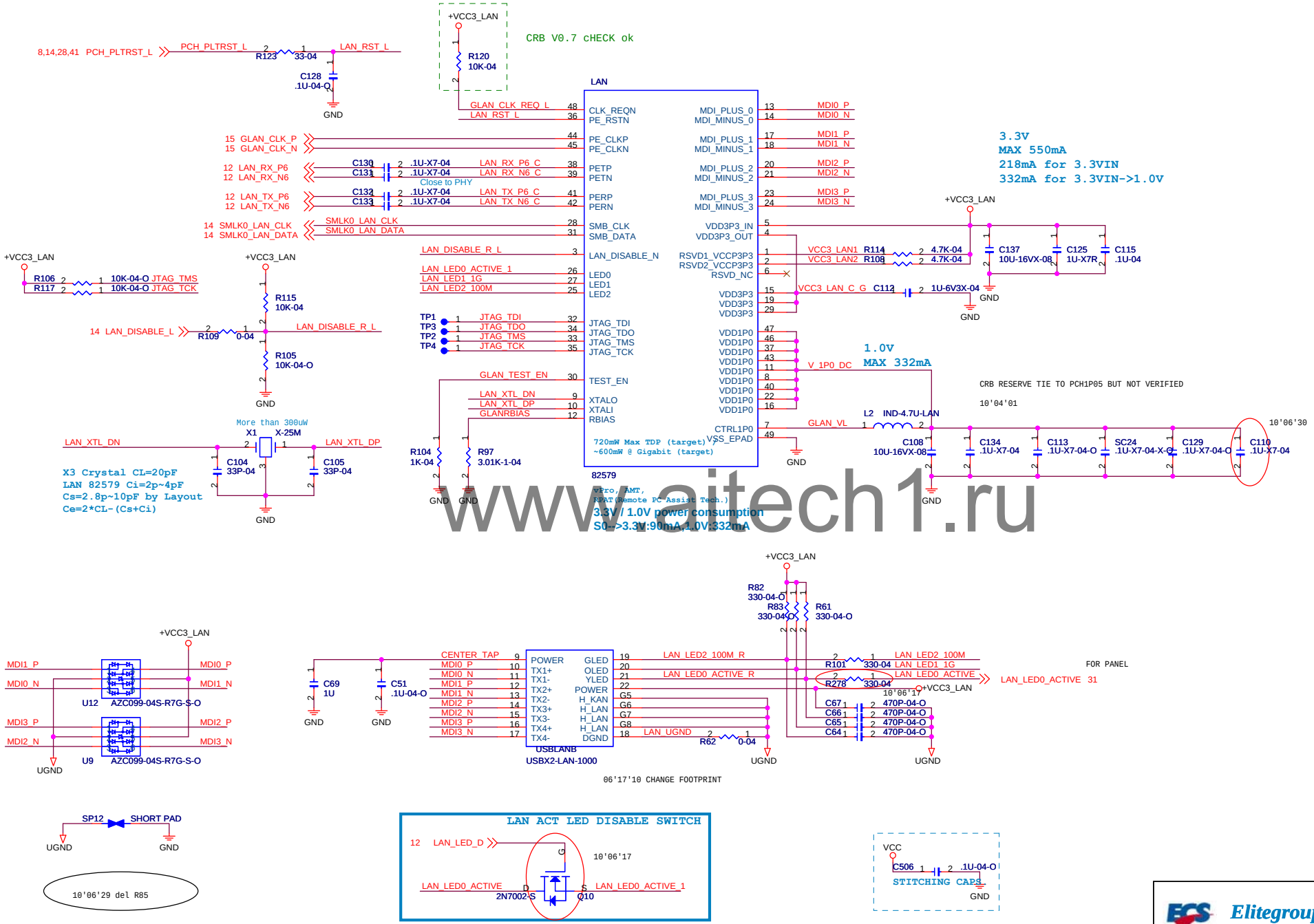
Title: SPI ROM, SMBUS

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 21 of 44



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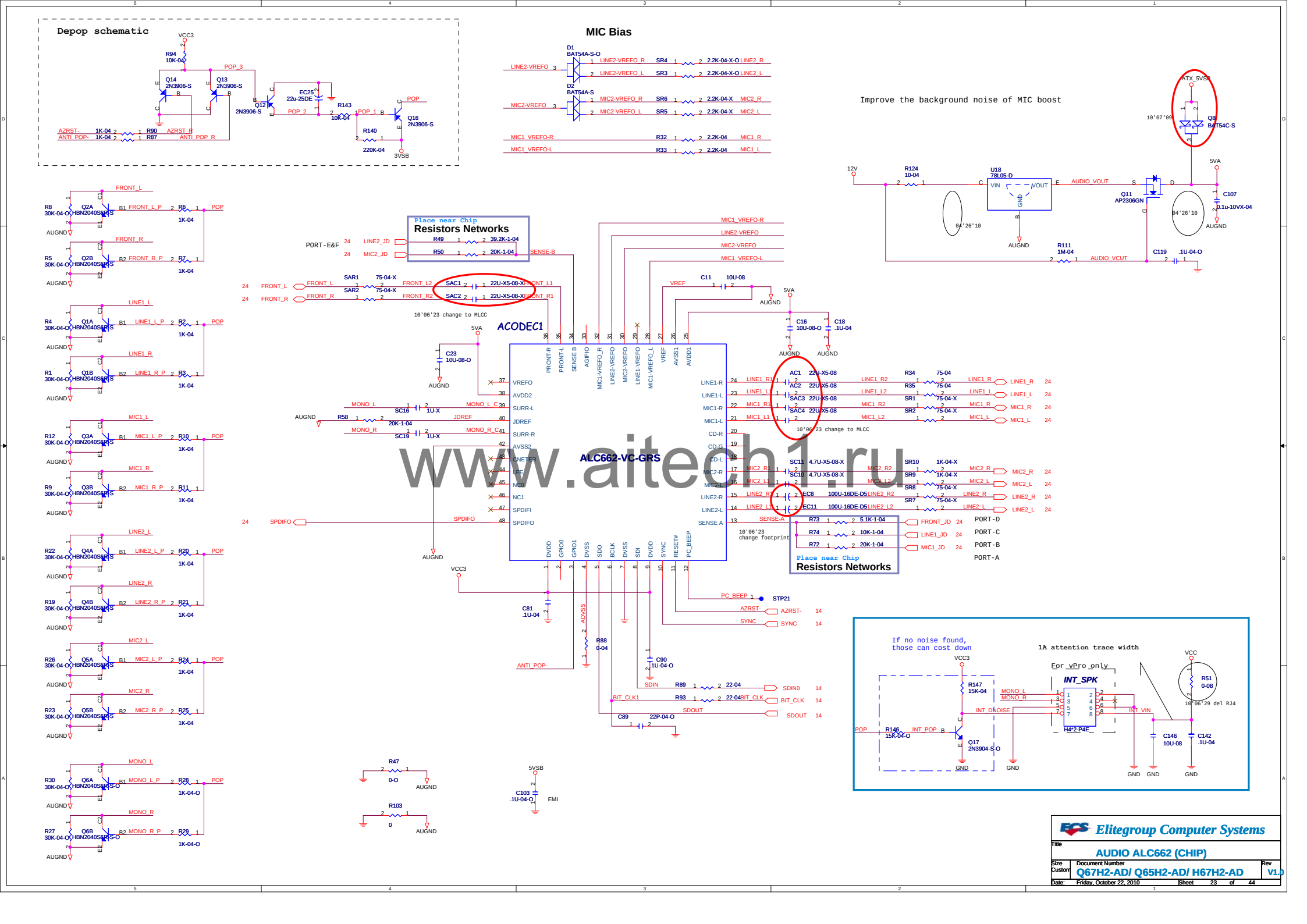
Elitegroup Computer Systems

Title: LAN PHY - 82579, USBLAN

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 22 of 44



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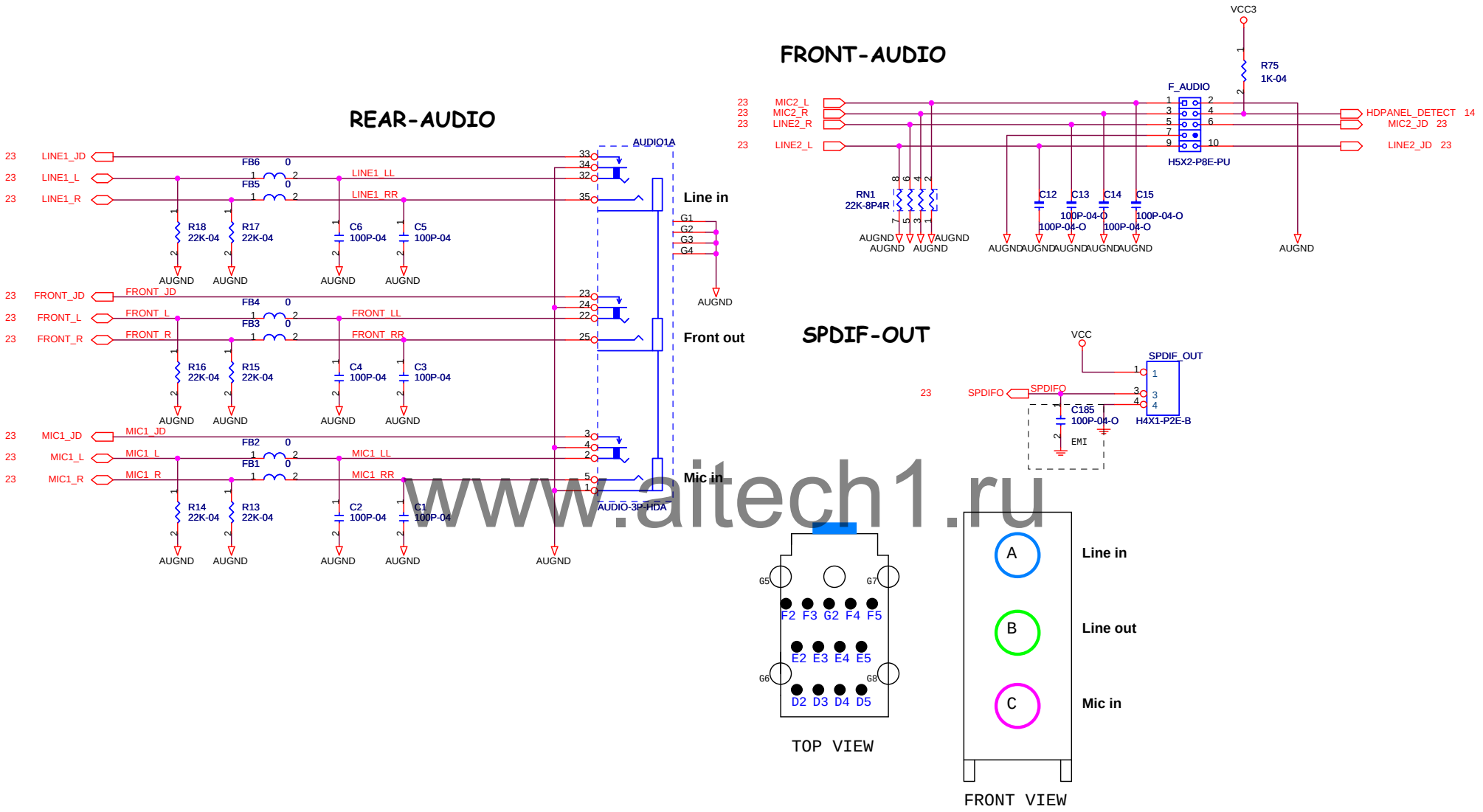

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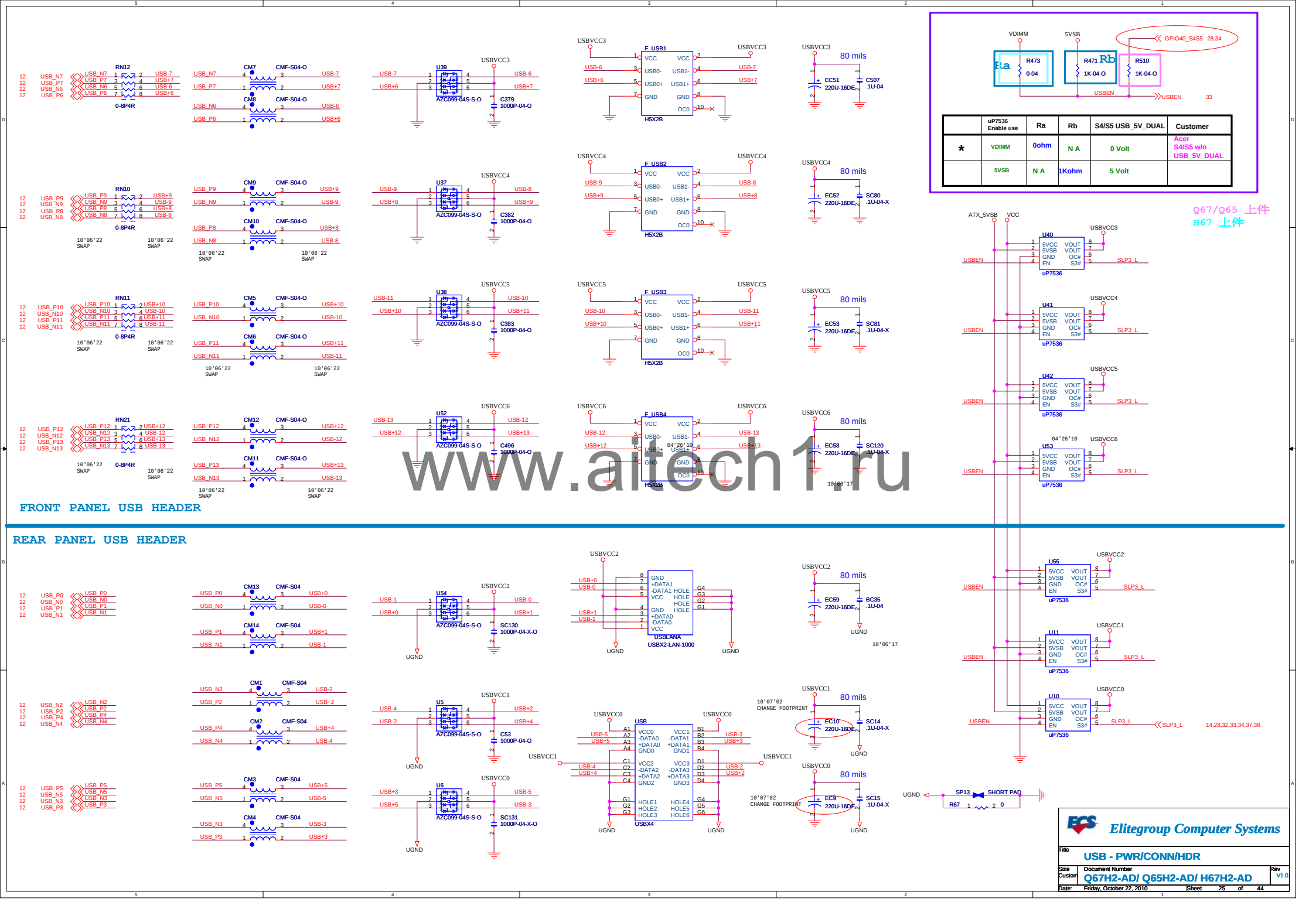
Elitegroup Computer Systems	
Title	AUDIO ALC662 (PANEL)
Size B	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD
Rev	V1.0
Date: Friday, October 22, 2010	Sheet 24 of 44



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Elitegroup Computer Systems

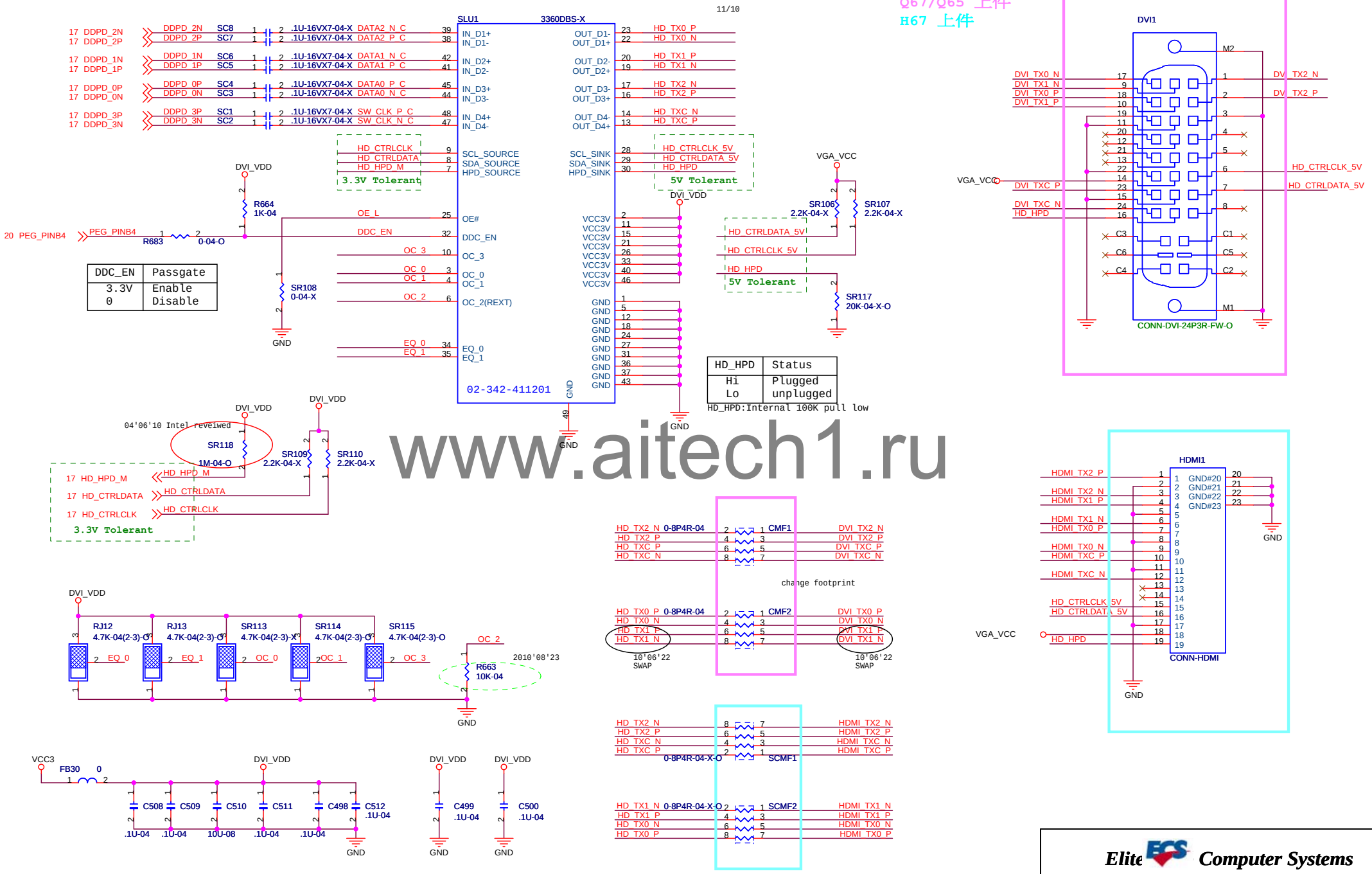
Title: USB - PWR/CONN/HDR

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 25 of 44

Level Shifter

Q67/Q65 上件
H67 上件



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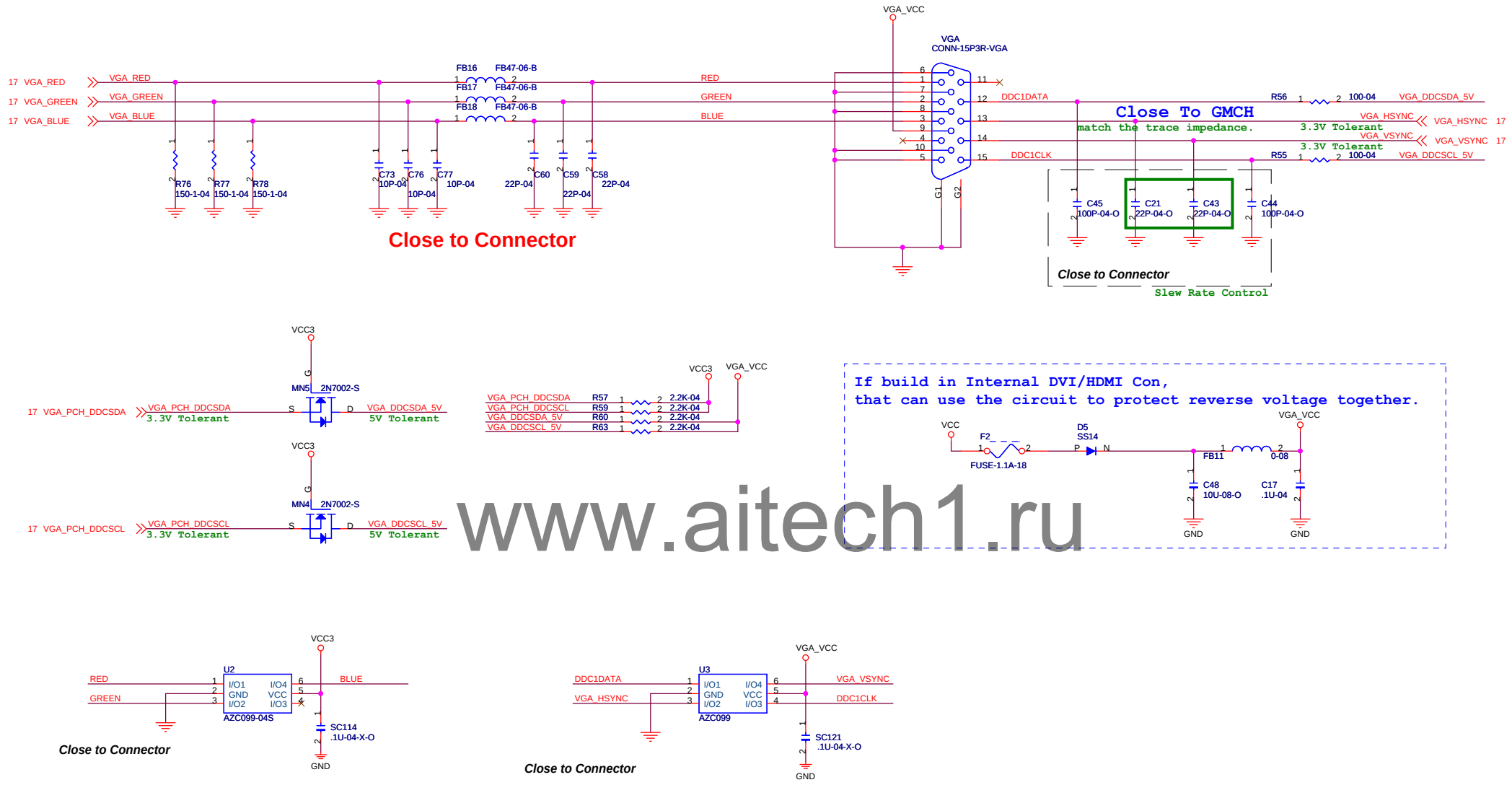
Elite ECS Computer Systems

Title: DVI HDMI(either one)

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 26 of 44



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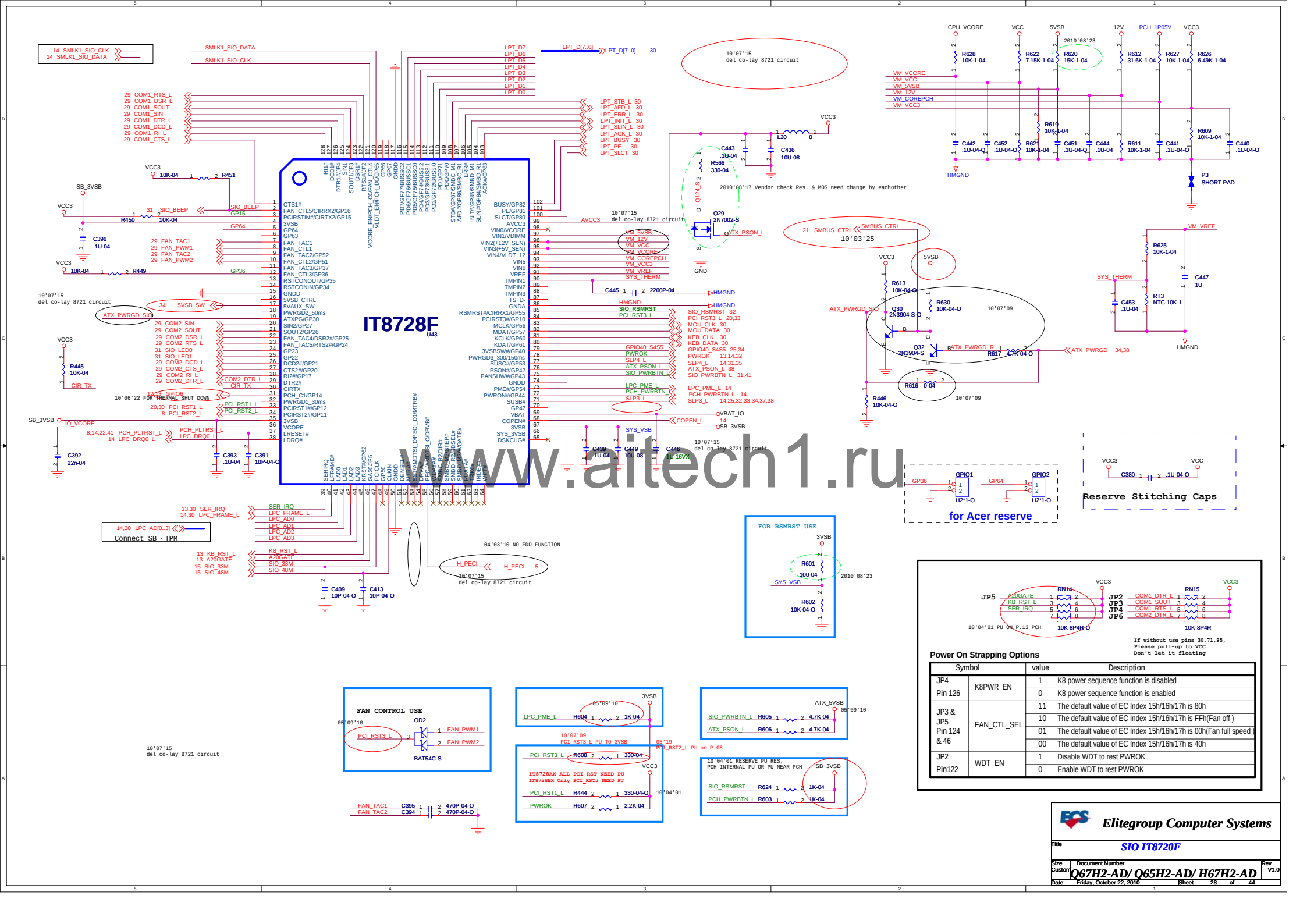
Elitegroup Computer Systems	
Title	VGA CONNECTOR
Size Custom	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD
Rev	V1.0
Date: Friday, October 22, 2010	Sheet 27 of 44



Symbol		value	Description
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 80h
		10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 40h
JP2 Pin122	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK

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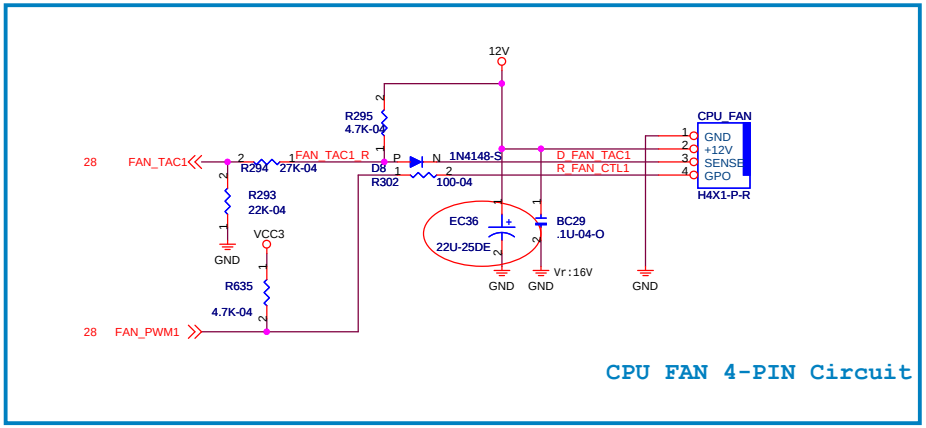
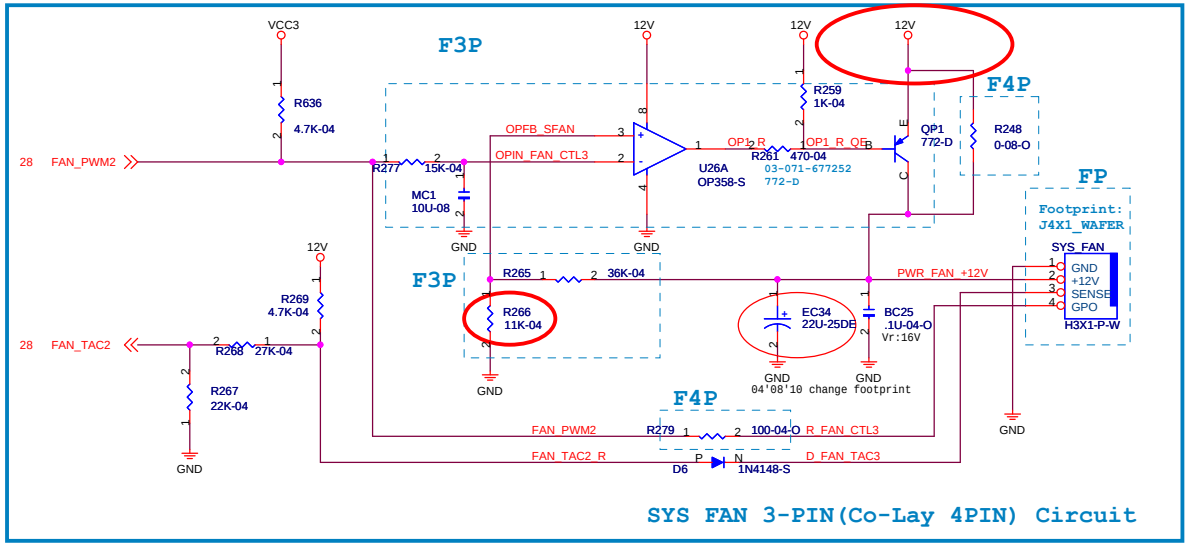
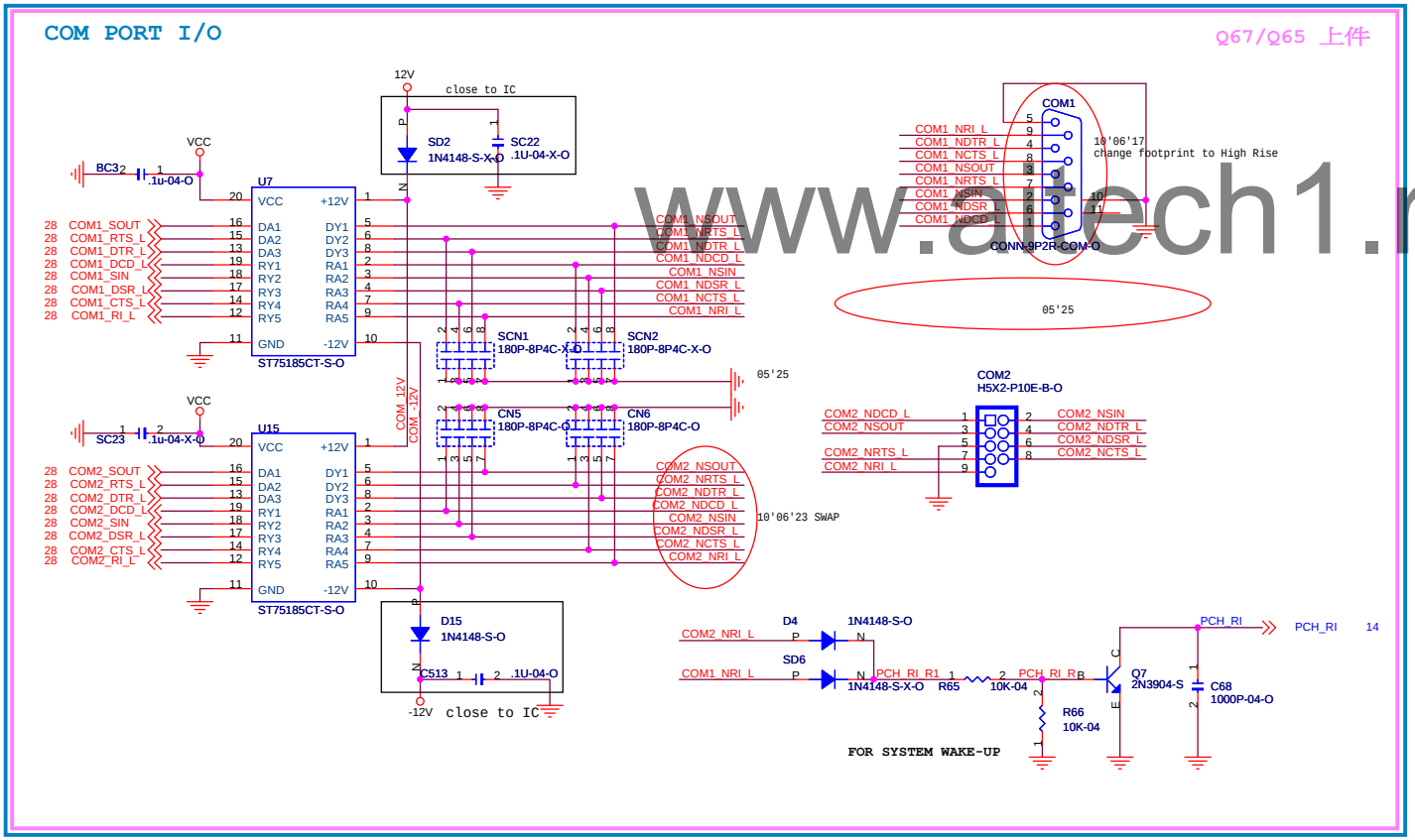




PWR FAN:

MODE	F3P	F4P	FP Value
* 3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W



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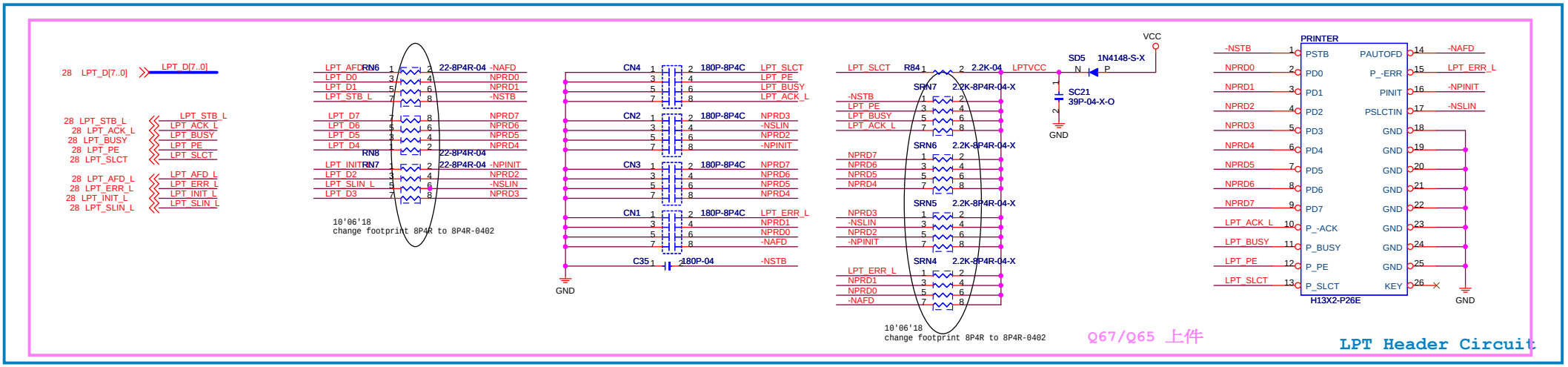
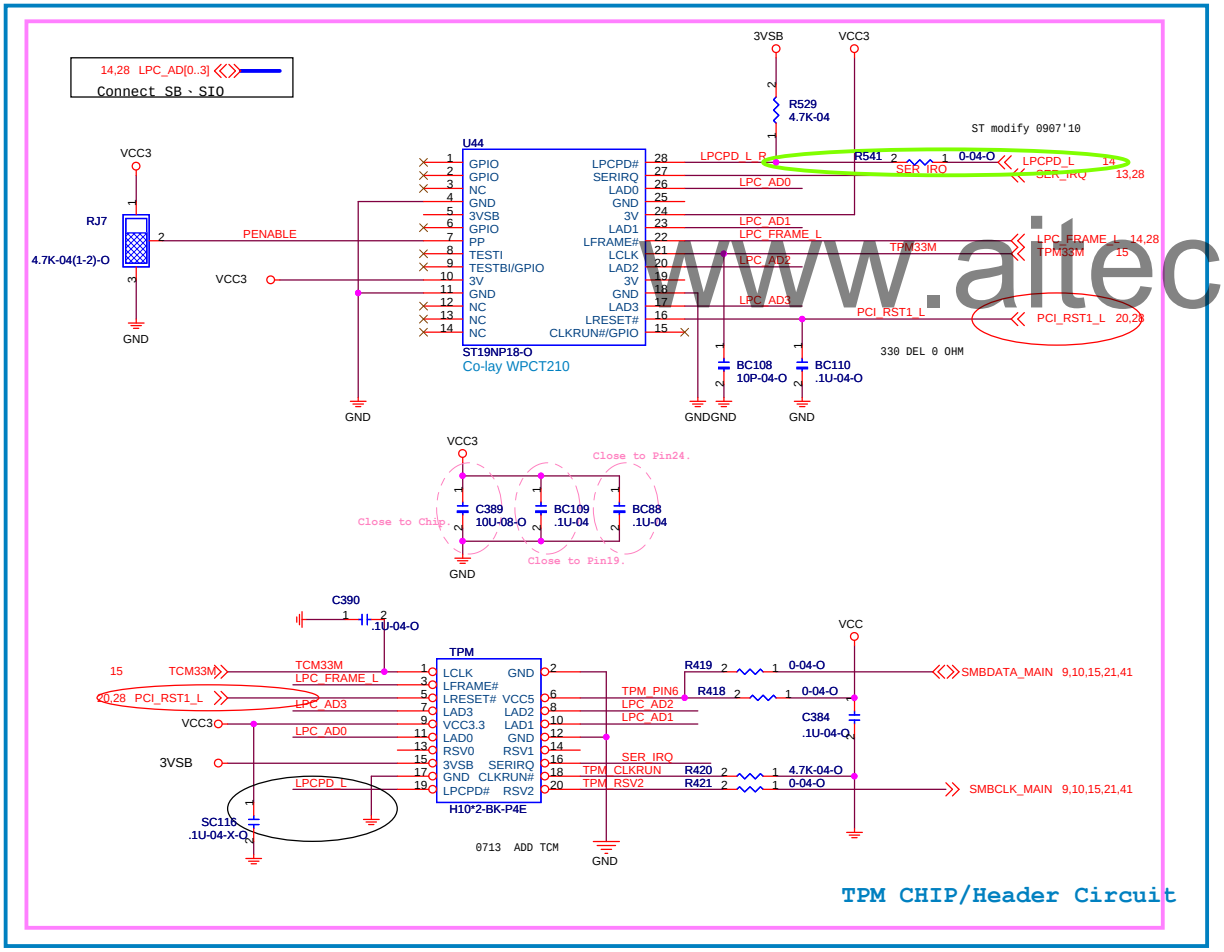
Elitegroup Computer Systems

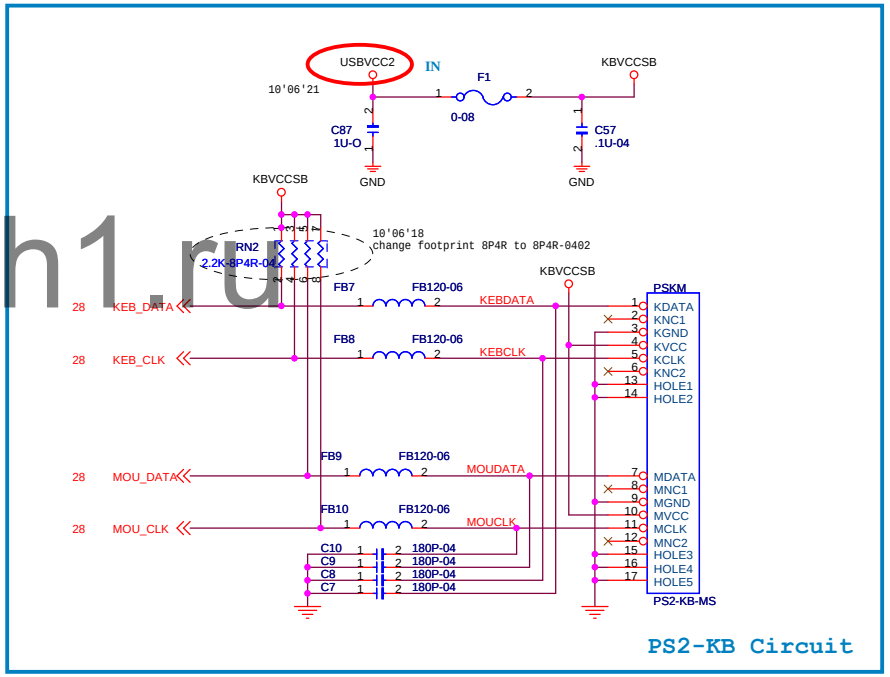
Title: FAN, COM

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 29 of 44







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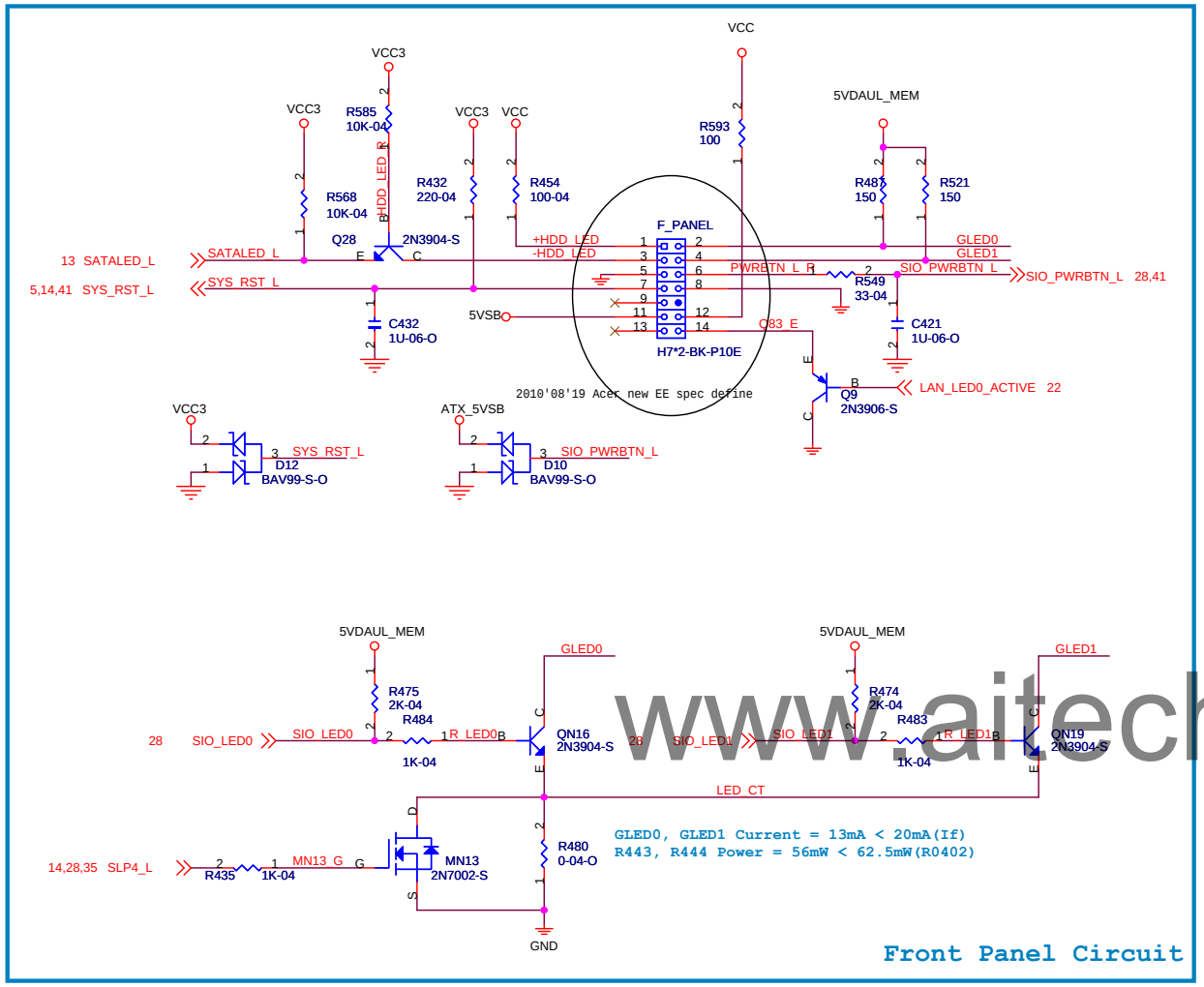
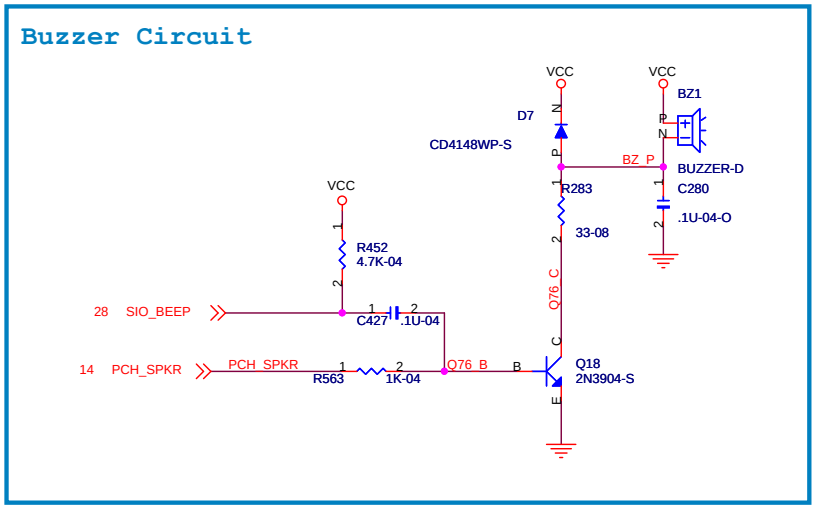
Elitegroup Computer Systems

Title: TPM, PS/2, LPT

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 30 of 44





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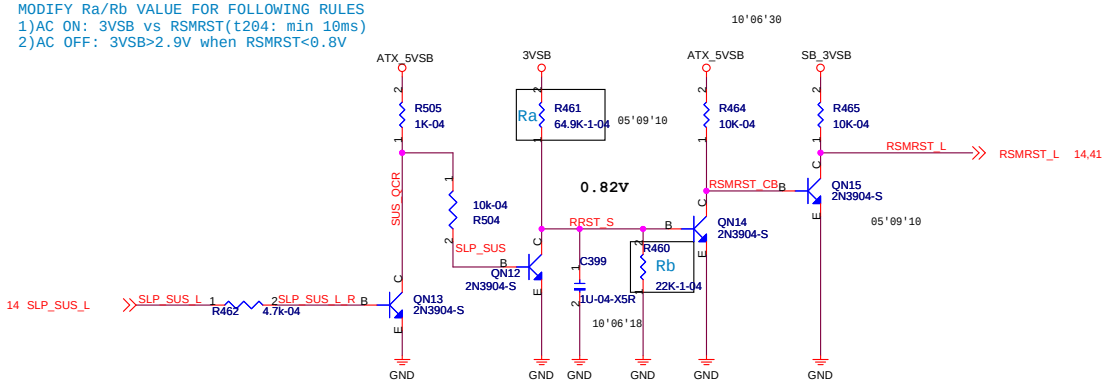
Elitegroup Computer Systems

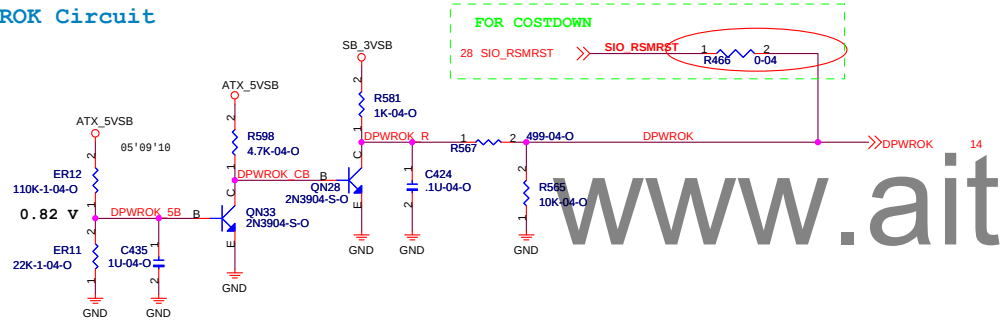
Title	F_PANEL, BUZ
Size B	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD
Rev	V1.0
Date: Friday, October 22, 2010	Sheet 31 of 44

RSMRST Circuit

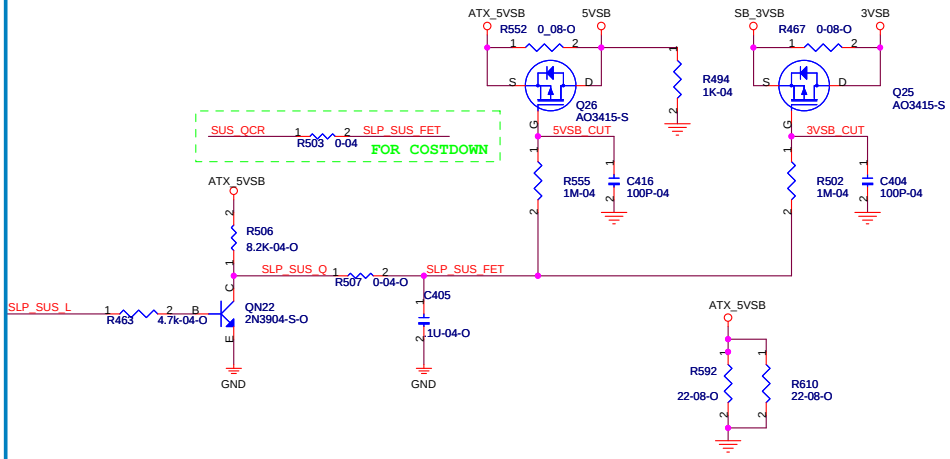
MODIFY Ra/Rb VALUE FOR FOLLOWING RULES
1)AC ON: 3VSB vs RSMRST(t204: min 10ms)
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V



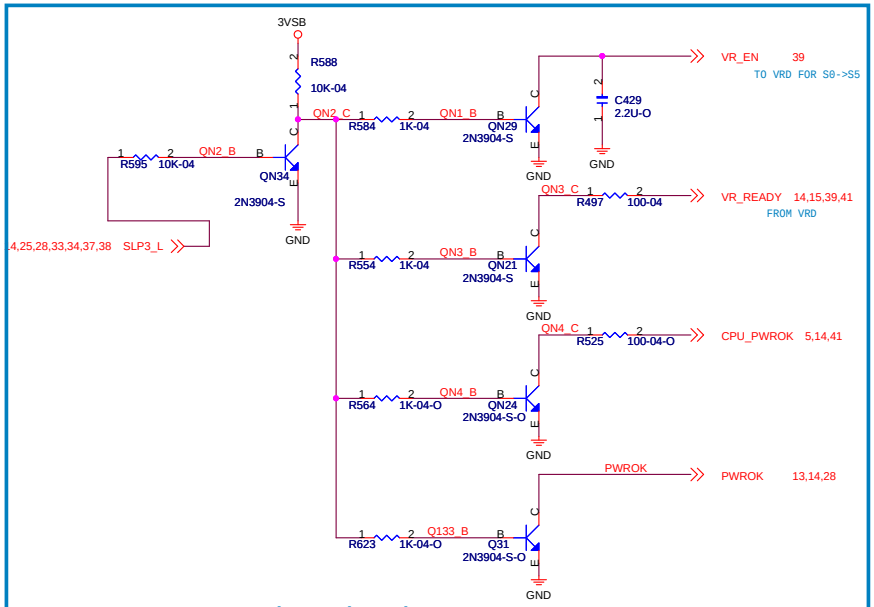
DPWROK Circuit



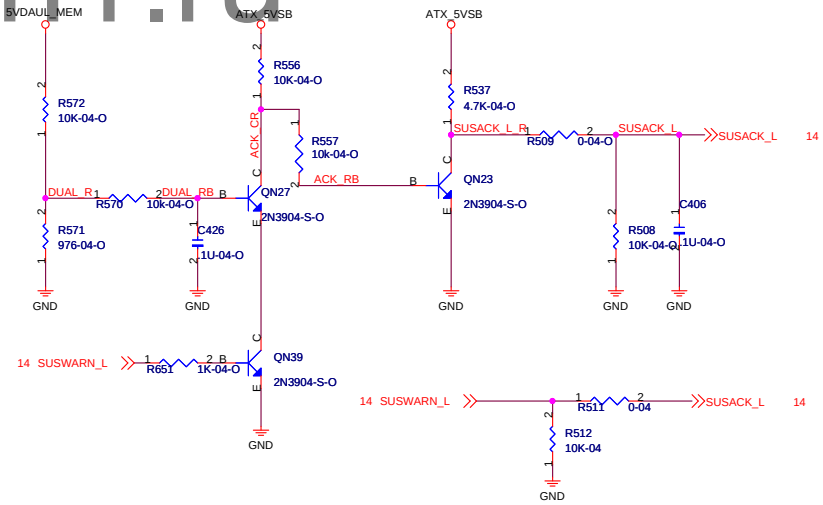
SUS_3/5VSB SWITCH



Power Down Sequencing Circuit



SUSACK_L CTRL CIRCUIT



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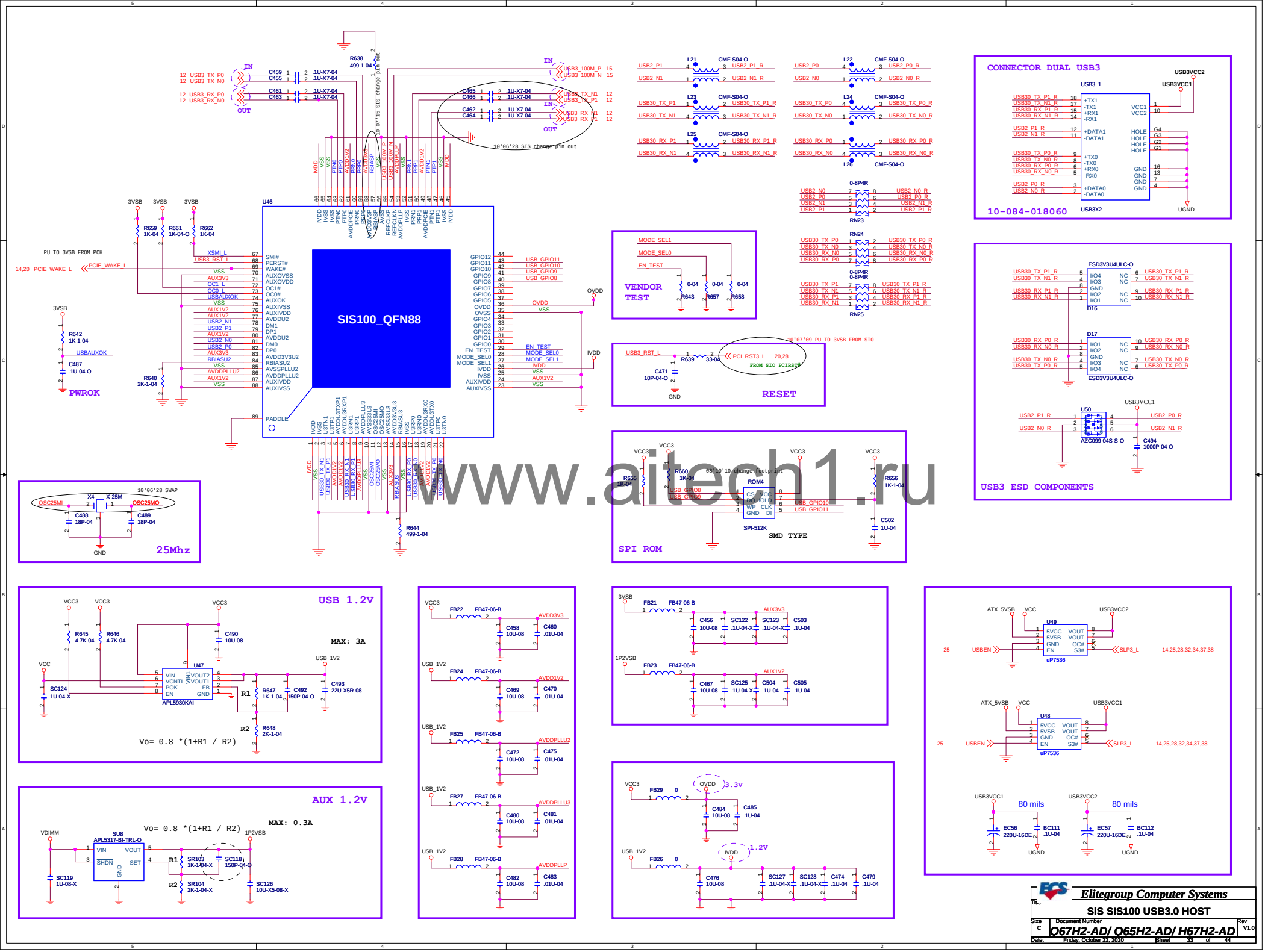
Elitegroup Computer Systems		
Title: SEQUENCE/ DSW CKT		
Size: Custom	Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD	Rev: V1.0
Date: Friday, October 22, 2010	Sheet 32 of 44	



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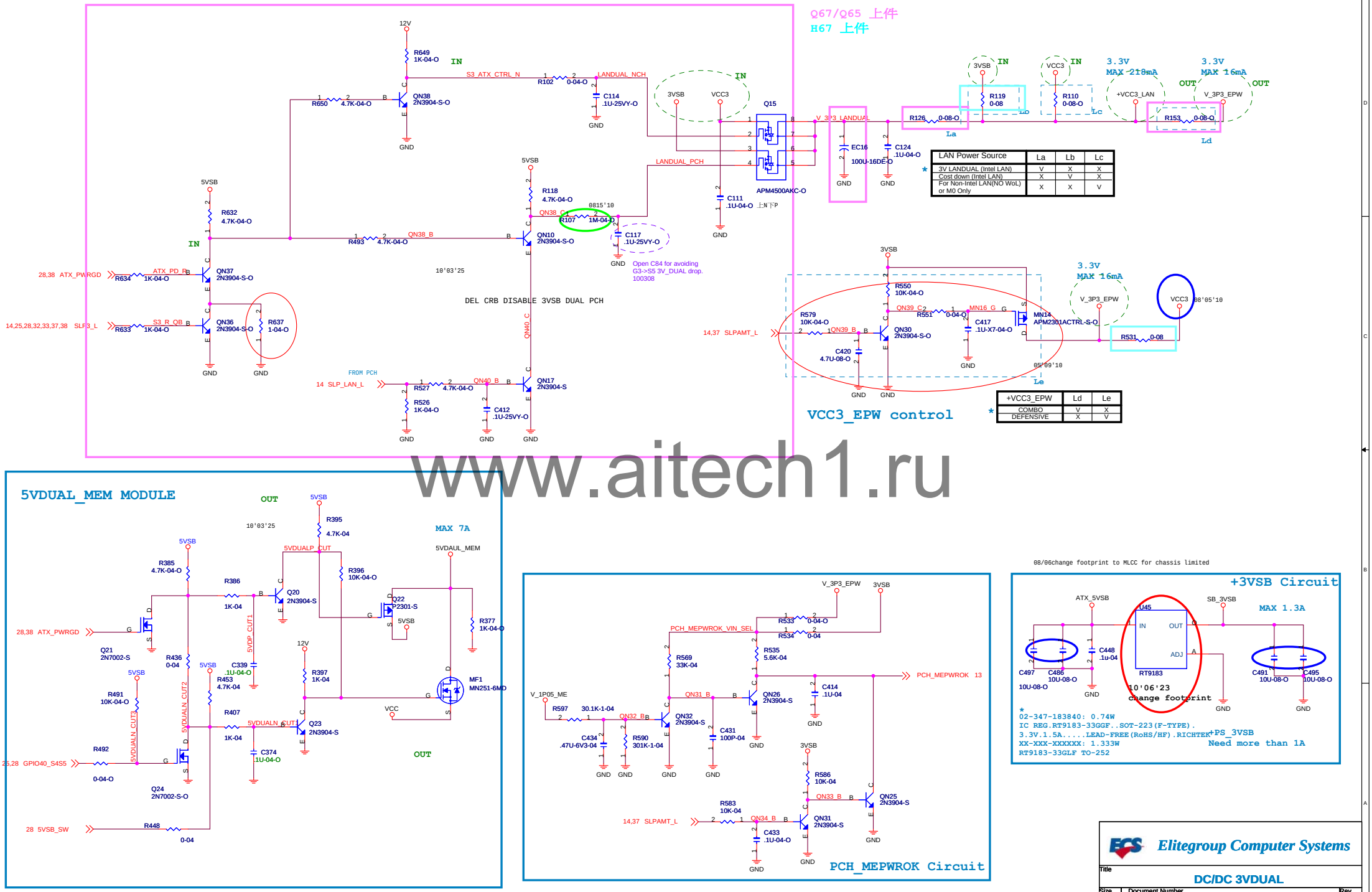
Elitegroup Computer Systems

Title: SiS SIS100 USB3.0 HOST

Size: C | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 33 of 44



LAN Power Source	La	Lb	Lc
3V LANDUAL (Intel LAN)	V	X	X
Cost down (Intel LAN)	X	V	X
For Non-Intel LAN(NO WoL) or M0 Only	X	X	V

+VCC3_EPW	Ld	Le
COMBO	V	X
DEFENSIVE	X	V

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VDIMM

SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.

02-436-587890
IC PWM.NCP1587DR2G..SO 8P.0.8V.....LEAD-FREE(RoHS).ON

Layout Note:
EC43, EC49.
Dual Value / Footprint:
560U-6V3OD6H9E / OSCON2D5_6D3_H9MM
560U-6.3D-OS-J / EC3D5_8_H9MM_1P

Layout Note:
VSMCx are under Channel B.
VSMCz are between Channel A & CPU.

MAX 28A
DCR=2mohm
08-413-105098
08-413-105099

1.5V
MAX 22A
VDIMM

10'07'02
CHANGE FOOTPRINT

20100705 CHANGE FOOTPRINT

loc=Iocset*Rocset/Rdson.
Iocset=10uA.

Ioc = 37~42A
Vgs = 4.5V
QML1//QML2 = 4m ~ 4.5m Ohm

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DDR_VTT

0326 NETLIST

CRB RESERVE S3 CTRL CKT

10'07'09
change footprint

0.75V
MAX 1A
VTT_DDR

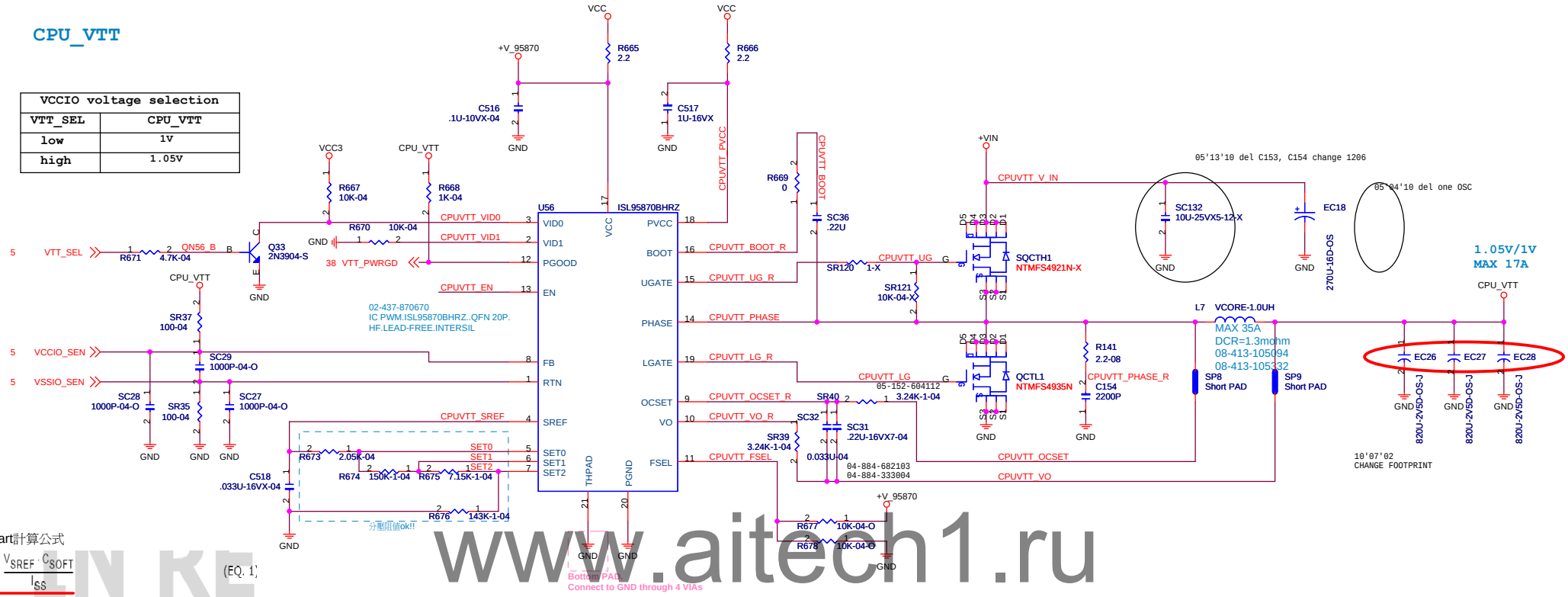
Layout Note:
SMVTTCf close to U35 Pin4.
SMVTTCg are between Channel A & B.
SMVTTCh are between Channel A & CPU.

Elitegroup Computer Systems

Title	DC/DC VDIMM/DDR_VTT/5VDUAL	
Size Custom	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD	Rev V1.0
Date: Friday, October 22, 2010	Sheet 35 of 44	

CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad \text{(EQ. 1)}$$

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

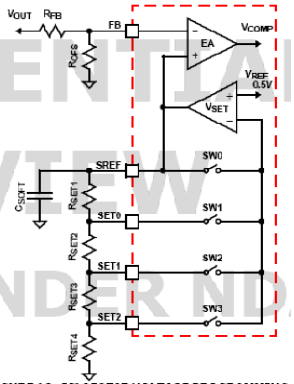
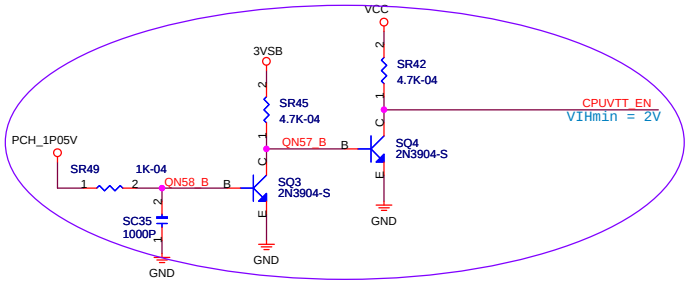


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT



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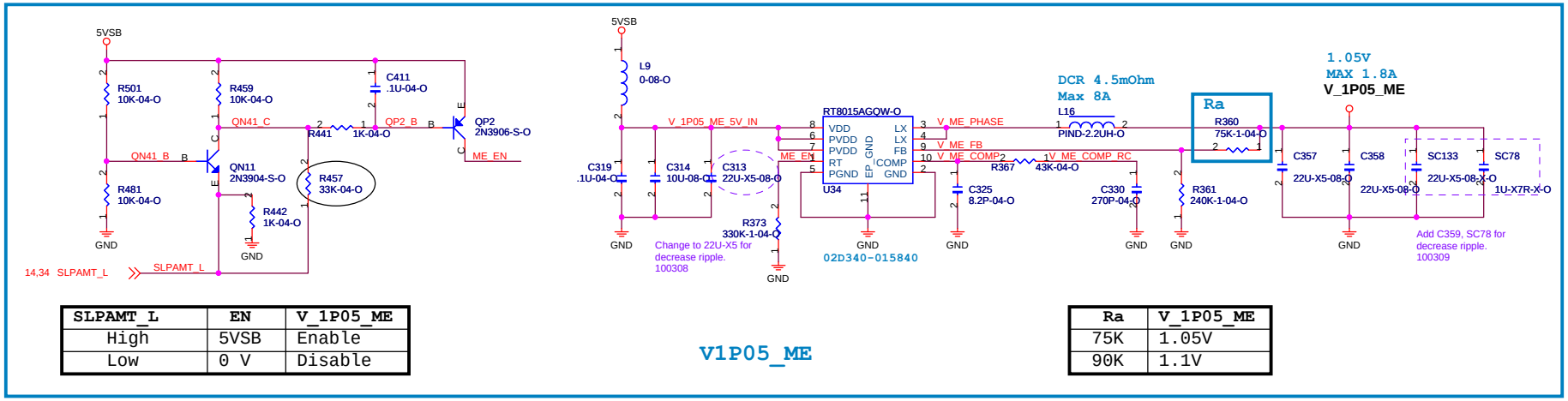
CONFIDENTIAL
IN REVIEW
RELEASE UNDER NDA

Elitegroup Computer Systems

Title: DC/DC V_CPUVTT

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

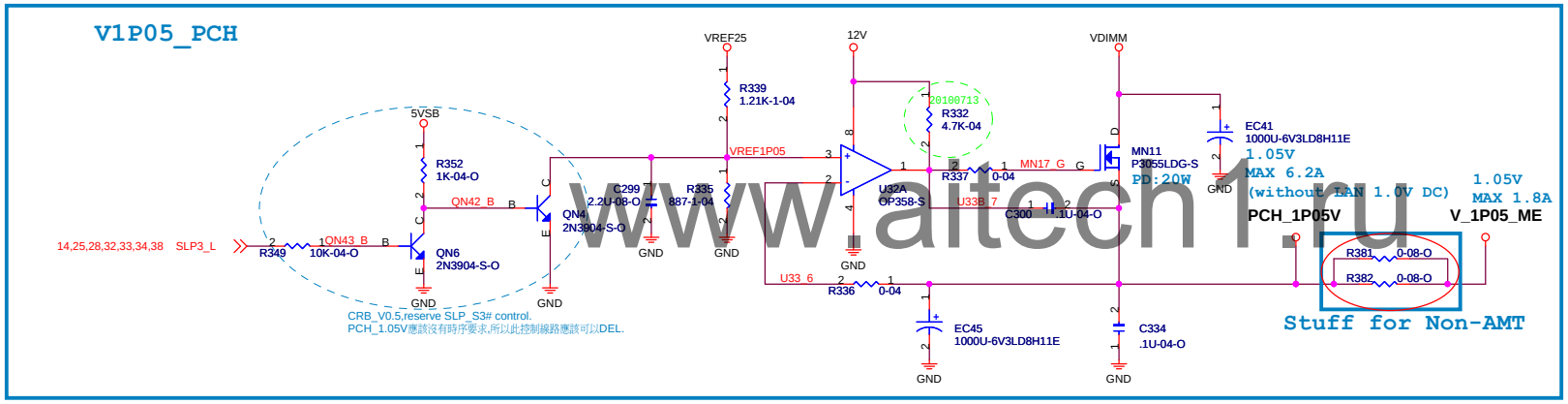
Date: Friday, October 22, 2010 | Sheet 36 of 44



SLPAMT_L	EN	V_1P05_ME
High	5VSB	Enable
Low	0 V	Disable

V1P05_ME

Ra	V_1P05_ME
75K	1.05V
90K	1.1V



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BOM Note:

02-340-015840....dfn10_rt8106a
IC REG.RT8015AGQW.WDFN 10P.3A.LEAD-FREE(RoHS/HF).
RICHTEK

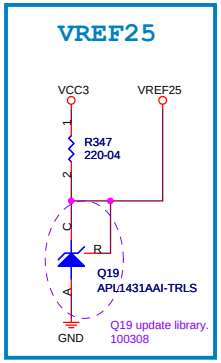
08-413-225094....choke_2r2m_pt4d9x4d6mm
POWER IND.2.2uH.20%.8A.4.5m OHM.DIP 2P.8.2*8.2*7.5*6.7 mm.AKL0806MN-2R2M-L3.2....LEAD-FREE(RoHS).MAGIC

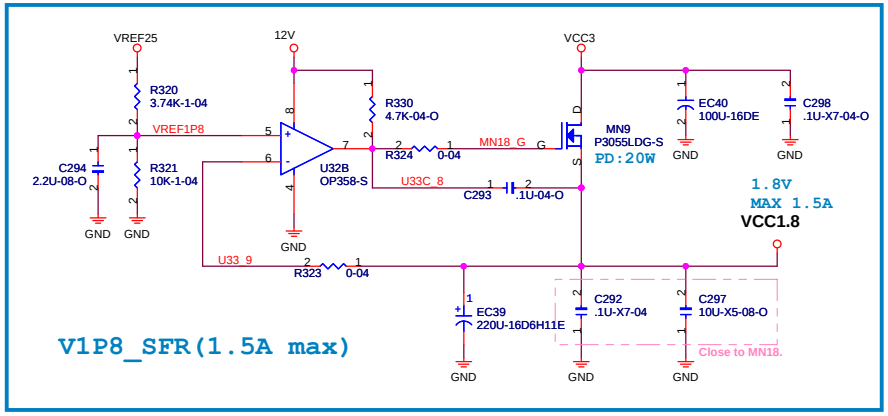
05-152-750113
RES.75K.1/16W.1%..SMD 0402.....LEAD-FREE(RoHS/HF).

05-152-430103
RES.43K.1/16W.5%..SMD 0402.....LEAD-FREE(RoHS/HF).

05-152-240114
RES.240K.1/16W.1%..SMD 0402.....LEAD-FREE(RoHS/HF).

04-880-828100
C/C.8.2pF.50V.0.25pf..NPO...SMD 0402....LEAD-FREE(RoHS/HF).





Elitegroup Computer Systems

Title	DC/DC V1P05_PCH,ME/V1P8_SFR	
Size Custom	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD	Rev V1.0
Date: Friday, October 22, 2010	Sheet 37 of 44	

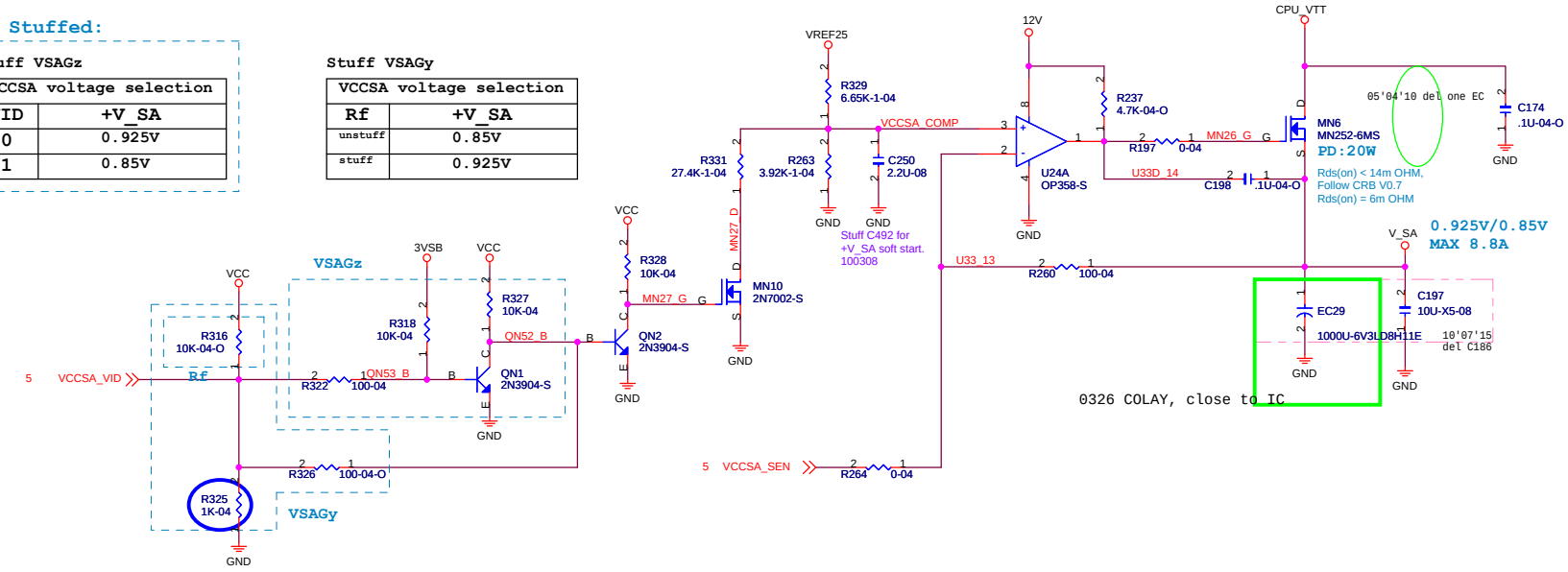
Default Stuffed:

Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
* 1	0.85V

Stuff VSAGy

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V



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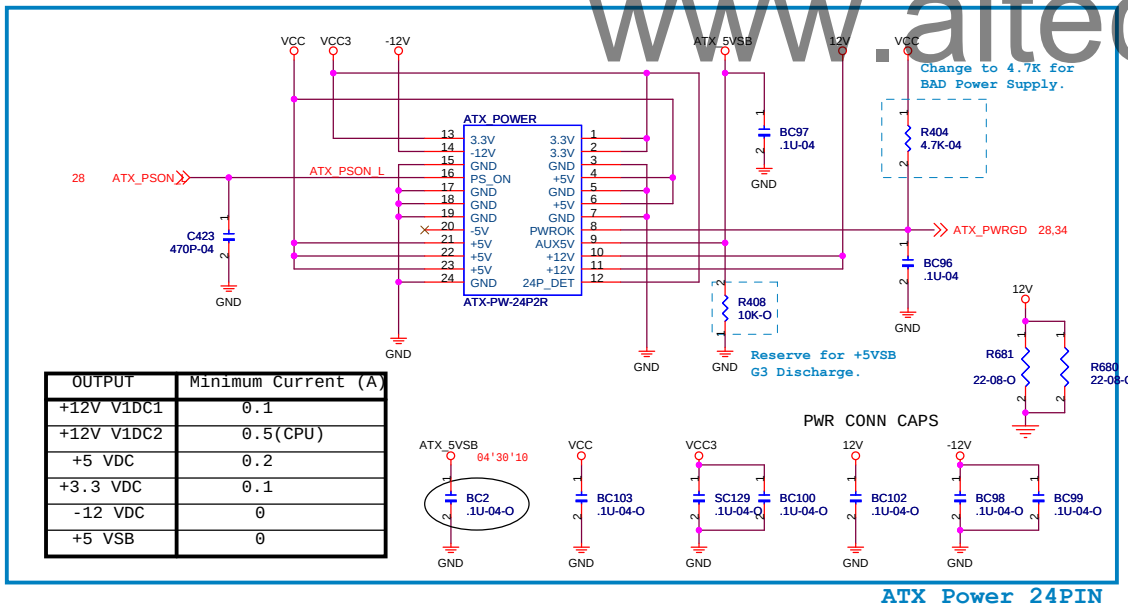
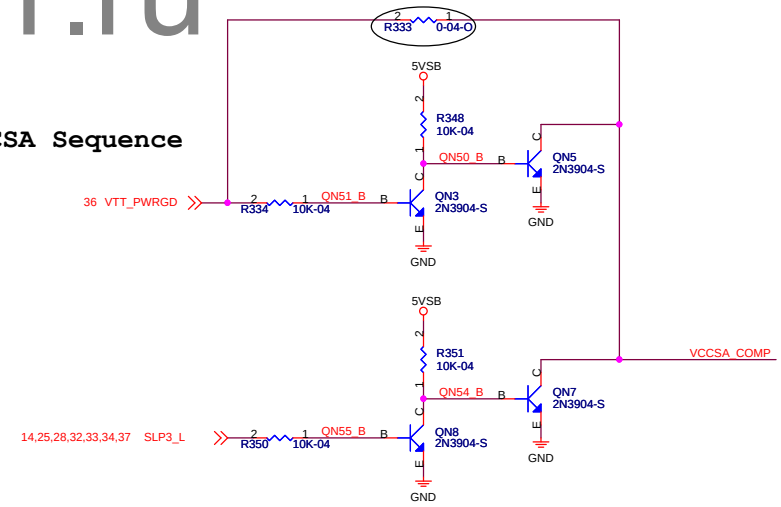


OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

PWR CONN CAPS

ATX Power 24PIN

VCCSA Sequence



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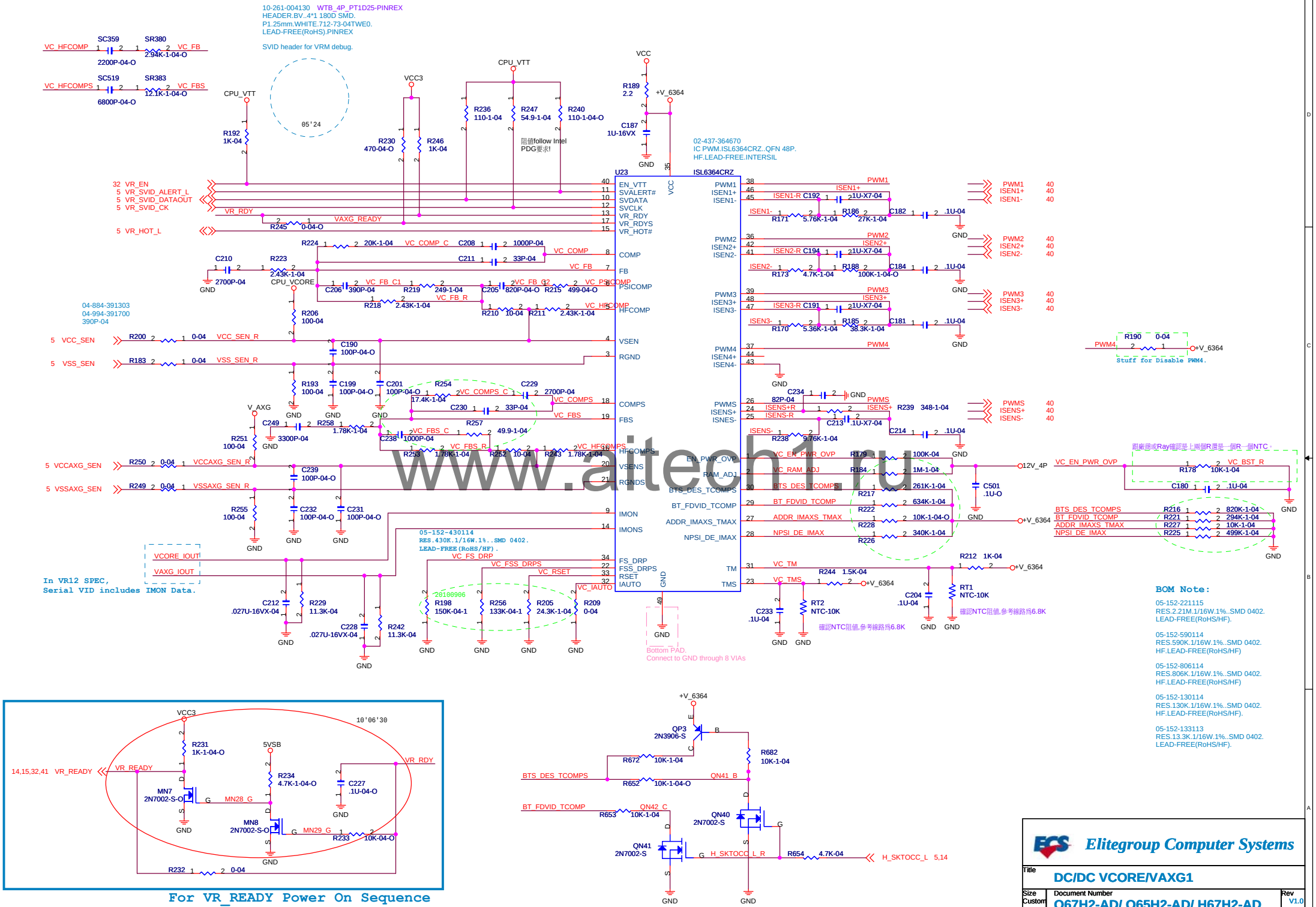
Title	DC/DC VCCSA, ATXPWR	
Size Custom	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD	Rev V1.0
Date: Friday, October 22, 2010	Sheet 38 of 44	


10-261-004130 WTB_4P_PT1D25-PINREX
HEADER.BV..4*1 180D SMD.
P1.25mm.WHITE.712-73-04TWE0.
LEAD-FREE(RoHS).PINREX
SVID header for VRM debug.
02-437-364670
IC PWM.ISL6364CRZ..QFN 48P.
HF.LEAD-FREE.INTERSIL
U23
ISL6364CRZ
阻值follow Intel PDG要求!
04-884-391303
04-994-391700
390P-04
Stuff for Disable PWM4.
跟廠商或Ray確認是上兩個R還是一個R一個NTC。
確認NTC阻值,參考線路為6.8K
05-152-430114
RES.430K.1/16W.1%..SMD 0402.
LEAD-FREE(RoHS/HF).
Bottom PAD.
Connect to GND through 8 VIAs
In VR12 SPEC,
Serial VID includes IMON Data.
BOM Note:
05-152-221115
RES.2.21M.1/16W.1%..SMD 0402.
LEAD-FREE(RoHS/HF).
05-152-590114
RES.590K.1/16W.1%..SMD 0402.
HF.LEAD-FREE(RoHS/HF)
05-152-806114
RES.806K.1/16W.1%..SMD 0402.
HF.LEAD-FREE(RoHS/HF)
05-152-130114
RES.130K.1/16W.1%..SMD 0402.
HF.LEAD-FREE(RoHS/HF).
05-152-133113
RES.13.3K.1/16W.1%..SMD 0402.
LEAD-FREE(RoHS/HF).
For VR_READY Power On Sequence
Elitegroup Computer Systems
Title
DC/DC VCORE/VAXG1
Size Custom
Document Number
Q67H2-AD/ Q65H2-AD/ H67H2-AD
Rev V1.0
Date: Friday, October 22, 2010
Sheet 39 of 44

**Vcore先4 phases上1下2,placement放不下再改3相上2下2.
**ISL6625明天Q1底才有sample,先用ISL6612CB.

02-415-612672
IC DRIVER.ISL6612ACBZ..SO 8P.LEAD-FREE.INTERSIL

0.65~1.3V
MAX 112A

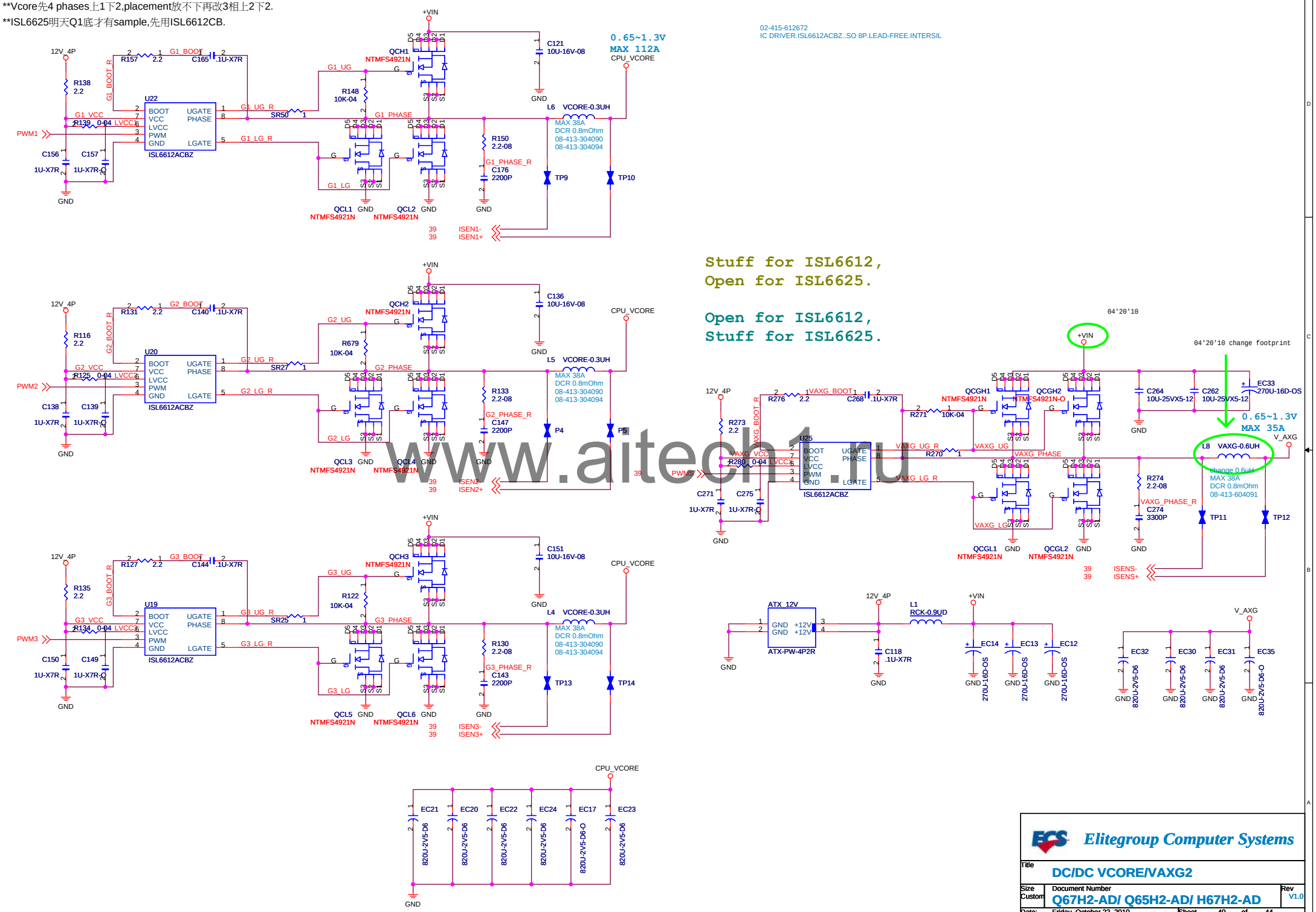
Stuff for ISL6612,
Open for ISL6625.

Open for ISL6612,
Stuff for ISL6625.

04'20'10

04'20'10 change footprint

0.65~1.3V
MAX 35A



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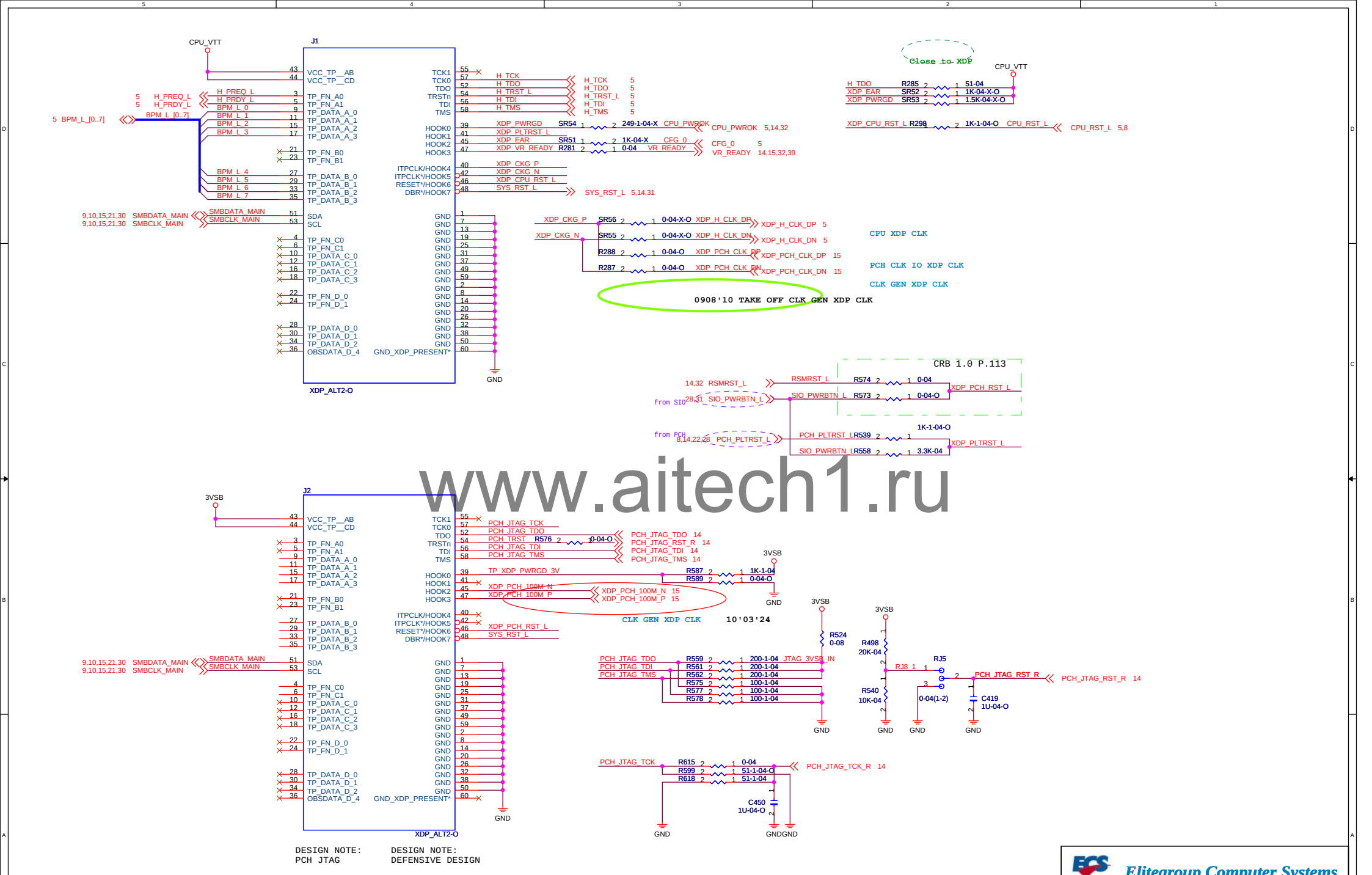
Title	DC/DC VCORE/VAXG2
Size Custom	Document Number Q67H2-AD/ Q65H2-AD/ H67H2-AD
Rev	V1.0
Date: Friday, October 22, 2010	Sheet 40 of 44



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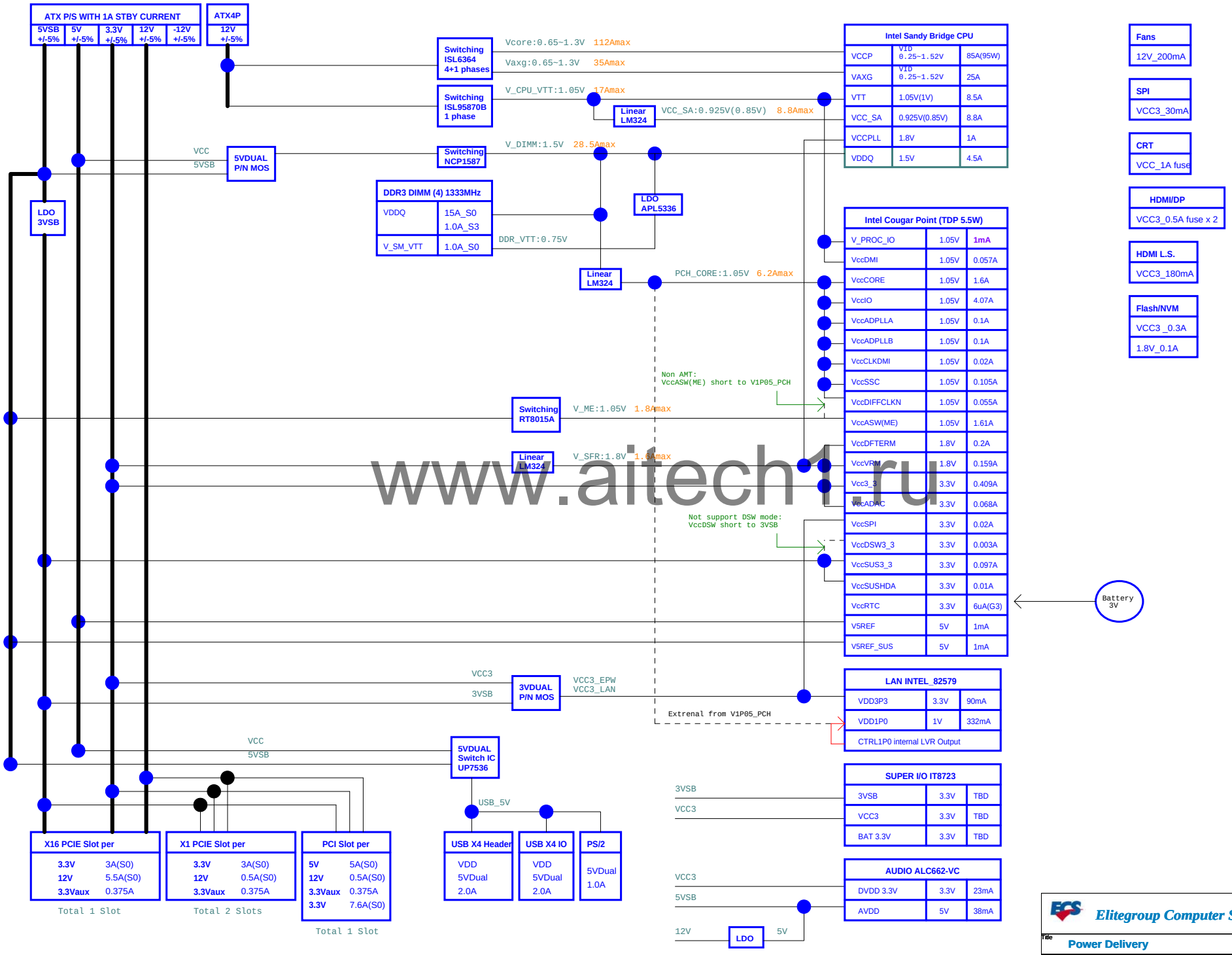

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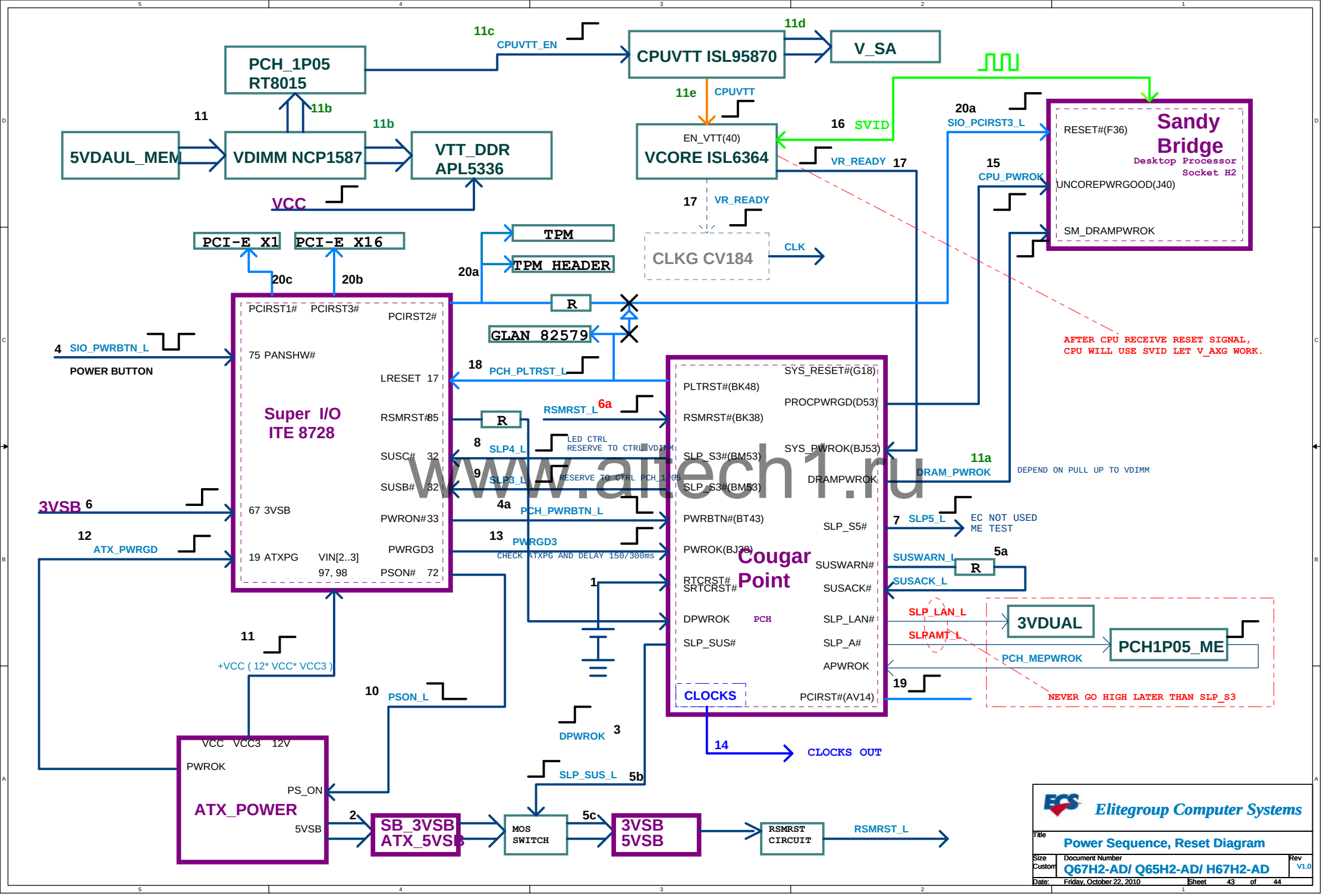
Title: Power Delivery

Size: C | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 42 of 44



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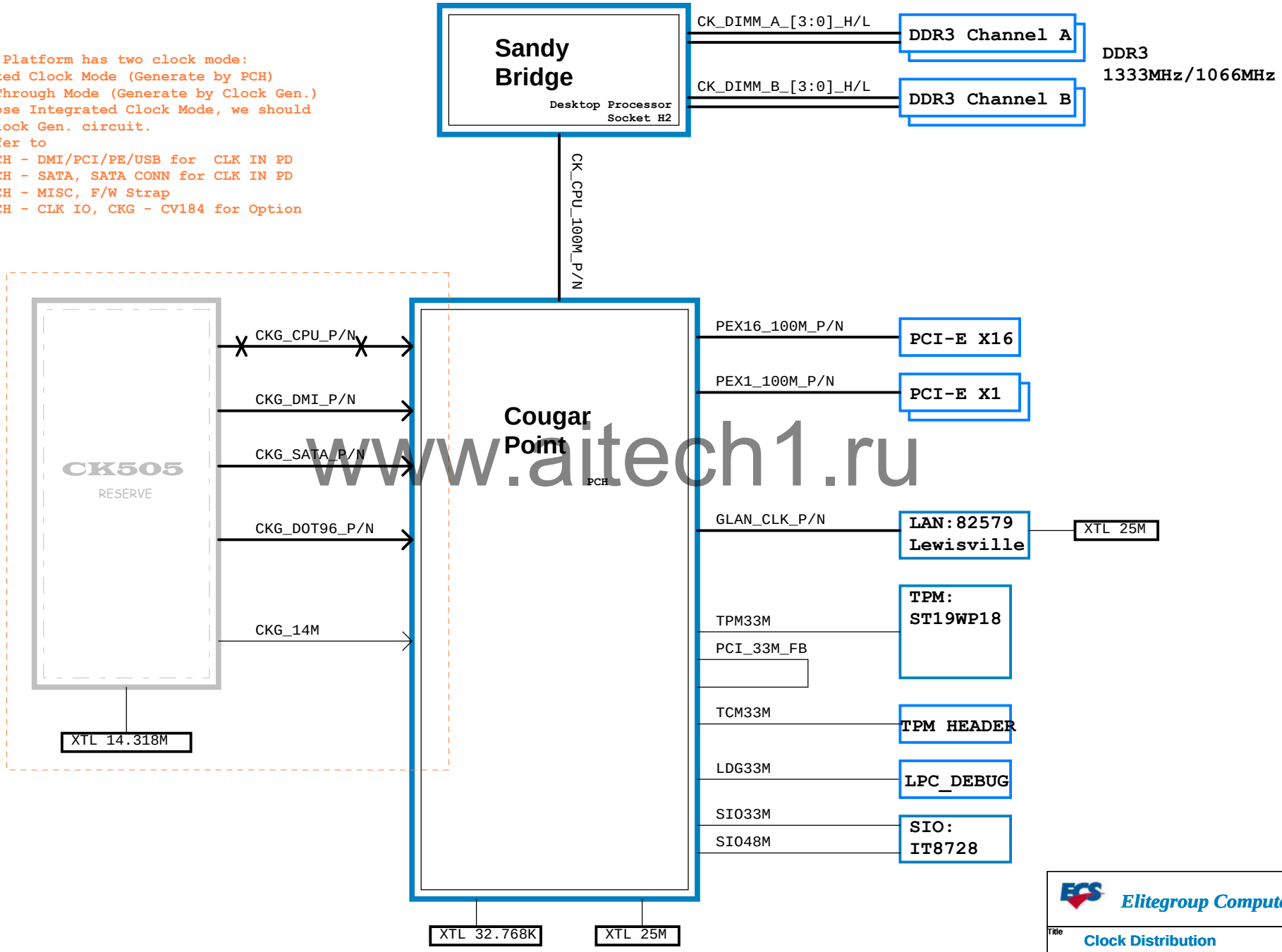
Title: Power Sequence, Reset Diagram

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 43 of 44

NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option



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Title: Clock Distribution

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

Date: Friday, October 22, 2010 | Sheet 44 of 44